Exhibit D
Part 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

____

EMC CORPORATION,

Petitioner,

v.

ACQIS LLC,

Patent Owner.

____

Case IPR2014-01462 (Patent 8,041,873 B2)

Case IPR2014-01469 (Patent RE42,814 E)

Thursday, August 27, 2015

Volume I of II

Deposition of VOLKER LINDENSTRUTH, taken at the offices of Gibson, Dunn & Crutcher, Carmelite House, 50 Victoria Embankment, London EC4Y 0DZ, beginning at 8:57 a.m. before Audrey Shirley, QRR, ACR, MBIVR.

EMC EXHIBIT 1028
EMC v. ACQIS, IPR2014-01462

A P P E A R A N C E S

FOR THE PETITIONER

GIBSON, DUNN & CRUTCHER LLP
1050 Connecticut Avenue, N.W.
Washington, DC 20036-5306
BY: BRIAN M. BUROKER, ESQ.,
Tel: +1 202 955 8541
Email: bburoker@gibsondunn.com

FOR THE PATENT OWNER

COOLEY LLP
380 Interlocken Crescent
Suite 900
Broomfield, Colorado 80021-8023
BY: BRITTON F. DAVIS, ESQ.,
Tel: +1 720 566 4126
Email: bdavis@cooley.com

I N D E X

Witness	Examination	Page
Volker Lindenstruth	(By Mr. Buroker)	4

E X H I B I T S

Exhibit No.	Description	Page
No. 1027	Document entitled "SCI implementation study for LHCb Data Acquisition."	99

VOLKER LINDENSTRUTH, having been duly sworn, was examined and testified as follows:

08:57:36

MR. BUROKER: For the record we should 08:57:36
probably announce ourselves. My name is Brian 08:57:38
Buroker from Gibson, Dunn & Crutcher, I represent 08:57:41
the petitioner in both proceedings, EMC. 08:57:42

MR. DAVIS: My name is Britton Davis, 08:57:47
I'm with Cooley LLP, I represent the patentholder 08:57:48
in both proceedings. 08:57:54

THE WITNESS: I am Volker Lindenstruth, 08:57:56
I am the witness. 08:57:58

EXAMINATION 08:58:00

BY MR. BUROKER: 08:58:00

Q. For the record, Dr. Lindenstruth, 08:58:00
would you please state your full name? 08:58:03

A. Professor Dr. Volker Lindenstruth, 08:58:05
born in Frankfurt 1962, October 8th. 08:58:07

Q. And please state your full 08:58:15
business address? 08:58:16

A. I have several business addresses. 08:58:23
The primary office is in Frankfurt, it is 08:58:26
Ruth-Moufang Street. "Ruth" as "Ruth" dash 08:58:31
M-o-u-f-a-n-g Street No. 1 in Frankfurt. The zip 08:58:40
code I don't remember off the top of my head. If 08:58:43

you want me to dig it out. 08:58:47
Q. I don't think that's necessary. 08:58:48
A. Second address would be GSI 08:58:51
Helmholtz Center in Darmstadt, Helmholtz with 08:58:54
T-Z, Planck Street 1, like Max Planck, zip code 08:59:02
again don't remember. 08:59:07
Q. And then for the record if you 08:59:08
would please state your home address? 08:59:10
A. This is Hoch Strasse, H-o-c-h 08:59:13
Strasse -- German word for street -- 84, 55128, 08:59:28
Mainz, M-a-i-n-z. 08:59:40
Q. And just so we're clear, this 08:59:41
deposition is being taken pursuant to two U.S. 08:59:46
Patent and Trademark Office proceedings related 08:59:50
to Inter Partes Review 2014-01469 and 08:59:57
IPR2014-01462. Is that your understanding, 09:00:07
Dr. Lindenstruth? 09:00:12
A. I believe so, I have the two here. 09:00:13
I don't remember the numbers off the top of my 09:00:16
head. One is the '873, 8,041,873 and the other 09:00:19
is the US RE42814. 09:00:23
Q. Right, those are the patent 09:00:34
numbers. If you look also on those documents 09:00:35
there's an IPR number and what I called out was 09:00:37
for the '814 Patent the IPR proceedings is 09:00:41

IPR2014-01469; is that correct? 09:00:45

A. Yeah. 09:00:49

Q. And for the '873 Patent, the IPR proceeding is IPR2014 01462; is that correct? 09:00:49 09:00:53

A. Okay, I didn't remember them therefore I just checked. 09:00:57 09:00:59

Q. And you understand that your testimony, although given here in the United Kingdom, is as if you were giving testimony in the United States, correct? 09:01:00 09:01:03 09:01:06 09:01:08

A. That's correct, yeah. 09:01:09

Q. And so that your testimony is subject to penalty of perjury under the United States law. Is that your understanding? 09:01:11 09:01:15 09:01:18

A. I understand that. 09:01:19

Q. Have you been deposed before? 09:01:20

A. In this kind of context, no. 09:01:23

Q. Is there another kind of context in which you have been deposed? 09:01:25 09:01:27

A. I have been involved in several cases of IP law where laws about compliance with certain products and so forth, but never in such a case, with a cross-examination. 09:01:29 09:01:31 09:01:39 09:01:43

Q. Were any of those cases related to court proceedings in the United States? 09:01:45 09:01:49

A. No. 09:01:51

Q. Were those cases involving court proceedings in Germany? 09:01:51 09:01:54

A. Leading to, yeah. But -- 09:01:57

Q. What do you mean -- well, were you finished? I'm sorry. 09:02:01 09:02:04

Well, let me step back a minute. Since you haven't been involved in a deposition, I'm sure your counsel went over this with you but let me explain the process and so forth. I'll ask a question and if you don't understand my question please let me know that you didn't understand it so I can clarify, is that fair? 09:02:04 09:02:07 09:02:10 09:02:13 09:02:16 09:02:18 09:02:21

A. Sure. 09:02:23

Q. If you don't say anything I'm going to assume you understood my question. The second thing is because this court reporter is doing a very good job and trying to keep track of the questions and answers, it's important that you wait for me to finish and I'll wait for you to finish your answer and I apologize I may have interrupted your last answer. So if you we can try to do that it will make everything easier on everybody involved, okay. 09:02:24 09:02:27 09:02:30 09:02:32 09:02:34 09:02:36 09:02:38 09:02:41 09:02:44 09:02:48

Is there any reason why you can't give 09:02:49

truthful testimony here today? 09:02:52
A. I'm not aware of any. 09:02:53
Q. No medications or anything that you may be taking that would impair your ability to testify truthfully? 09:02:54 09:02:56 09:02:58
A. No. 09:03:00
Q. Okay. So going back, what is the nature of the proceedings in which you have given testimony in the past? 09:03:00 09:03:07 09:03:10
A. Most cases are in the context of, for example, we are spending a lot of money buying computers, you have the public tender, you set forth documents, what the product has to comply with, product not being delivered and not being delivered according to spec and then you get into a fight with a vendor and normally it's being resolved, sometimes not, and then you prepare your way to the court. That's one example. 09:03:13 09:03:18 09:03:24 09:03:29 09:03:31 09:03:35 09:03:37 09:03:41 09:03:45 09:03:47
Another example, product being delivered and then turns out that there is a patent by another vendor which prevents this product from being used which of course is not a funny thing to be once you've paid the product already, and we're talking usually minimum €100,000 and more. 09:03:48 09:03:50 09:03:54 09:03:57 09:03:59 09:04:03

And then you prepare the case. 09:04:08
In most cases we could avoid going all 09:04:12
the way and settled one or the other way but, of 09:04:16
course, in order to get such a case without you 09:04:20
have to prepare it as if it was to go to court. 09:04:25
Q. So, breaking that down a little 09:04:30
bit, you have been involved in cases in which 09:04:34
companies or businesses you've been involved with 09:04:37
were accused of patent infringement; is that 09:04:40
correct? 09:04:43
A. In this one case there was no 09:04:45
direct infringement case yet raised, but I had 09:04:50
purchased a product for close to €200,000 where 09:04:53
subsequently the patent was issued in Germany 09:04:58
which prevented us to use that product. Since we 09:05:02
are public sector we can't just ignore the 09:05:05
existence of a patent and wait for the injunction 09:05:08
by the patent owner to stop us, right? I mean we 09:05:11
have high standards being the government. So 09:05:15
that had to be resolved. 09:05:18
Q. And in that proceeding did you 09:05:20
give testimony in court? 09:05:22
A. It didn't get that far 09:05:23
fortunately -- 09:05:25
Q. Have you -- 09:05:26

A. -- that case.

Q. Oh sorry. Have you given testimony in court proceedings anywhere in the world before?

A. Once in Germany that was a suit introduced by the University of Heidelberg against somebody who basically copied an entire class I did into a book under his own name, which obviously was not a good thing to happen, in particular because then later I had students argue that I plagiarized the authors of that particular book. That was the moment when I said that had to stop. The publishing house refused to do any remedy, so it went to court, the full proceeding. And since this is a -- the judge made it absolutely clear that this was plagiarism, but since this is about teaching and textbooks, in Germany there is a law which says knowledge must not be prevented from being taught by any copyrights. So he could not say whether or not by destroying that book he would prevent the teaching inside the book as the abstract teaching from still being taught. The judge suggested that we take this to the Supreme Court because that was an open case for Germany, which

the university wouldn't do for cost, and the case was settled that the publishing house committed to not selling this book -- only selling the already printed versions and signed a document that this book was an infringement -- was plagiarism, which was enough for me because then I could clearly document that I wasn't the one doing this. But this was an entirely different kind of proceeding like we have here. 09:07:04 09:07:08 09:07:13 09:07:16 09:07:18 09:07:23 09:07:25 09:07:28 09:07:31

Q. Right. So in that case you were testifying as a fact witness, a person of knowledge of the facts as opposed to an expert witness; is that correct? 09:07:35 09:07:37 09:07:41 09:07:44

A. So to say, yeah. 09:07:45

Q. Have you ever testified as an expert in any proceedings anywhere in the world? 09:07:47 09:07:49 09:07:53

A. Like this, no. 09:07:53

Q. Sir, when were you engaged to assist Acqis in connection with these proceedings? 09:07:54 09:08:00 09:08:05

A. This is quite a while ago. I believe roughly October last year, September, October last year, the exact date I do not remember. If you wish to have that date I would 09:08:07 09:08:10 09:08:18 09:08:21

have to go through my email records which I don't have here. I could give this to you later.

Q. Have you assisted Acqis in connection with any of the pending litigation matters as opposed to these two IPR proceedings?

A. No. Not as far as these documents go or anything, no.

Q. Have you reviewed any confidential information of the petitioner EMC that was produced in the litigation?

A. No.

Q. Have you reviewed any confidential information of Alcatel-Lucent from the Acqis-Alcatel-Lucent litigation?

A. I am not aware having seen that or even having heard about that. I am aware that there are things like that ongoing, but this is entirely out of the scope of my work here and the context in which we performed that work.

Q. Right and I'm just trying to get an understanding of what you did or didn't review since your engagement, so that's why I asked the question whether you had reviewed any confidential information of either EMC or Alcatel-Lucent. And so the answer is no, you

have not? 09:09:48

A. But for my understanding this is confidential information, it would be not even okay to give it to me, right? 09:09:49 09:09:51 09:09:54

Q. Well ... 09:09:59

A. You're kind of asking me whether I wrongfully saw a document. 09:10:01 09:10:03

Q. No, there are Protective Orders in the litigation that enable experts engaged by Acqis to see information, and we're not aware that you were provided information, but that's why I wanted to confirm you were not provided information under the terms of that Protective Order? 09:10:04 09:10:06 09:10:10 09:10:14 09:10:17 09:10:19 09:10:21

A. No. 09:10:24

Q. No. 09:10:25

(Brief off-the-record discussion.) 09:12:49

BY MR. BUROKER: 09:12:54

Q. It looks like you've got copies, and maybe these are the exact same things, but I was going to provide you copies with -- 09:12:54 09:12:56 09:12:58

A. Then I will take both, that's fine. 09:12:58 09:12:58

Q. -- Acqis Exhibit 2021 in both proceedings, so there's two different documents 09:13:01 09:13:04

but it's 2021 from the 1469 proceeding and 2021 from the 1462 proceeding as well. And I think they're probably the same as what you have.

Do you need a copy?

MR. DAVIS: Do you have the super nice bound one? If you do, I would love that. Thank you.

MR. BUROKER: I don't know how nice they are, but ...

MR. DAVIS: Thank you.

BY MR. BUROKER:

Q. So you recognize these two documents as printouts of the declaration that you signed and submitted in connection with the two proceedings? And I'm not giving you a - test. I'll represent that we believe they're full copies of each.

A. With this disclaimer absolutely, yes, I recognize them.

Q. How were these documents drafted? Did you write all the words in the document?

A. I did not write all the words in there, hardly ever do that. I mean I've reviewed all the material and we have come to conclusions, there have been discussions with Cooley and the

documents were jointly written. I have reviewed them several times very carefully, I have read them, both of them, all 250 altogether pages. Let me see the first one is about, I believe, roughly 100 pages, 93, plus an appendix, the other is 114, something like that, 111. I carefully read them to make sure that everything in there is correct and I still believe so today except for some very minor typos which we found, a few commas and so forth, nothing which really has any effect on the content of these documents. 09:14:41 09:14:44 09:14:47 09:14:52 09:14:54 09:14:59 09:15:03 09:15:07 09:15:12 09:15:16 09:15:20

Q. So you worked together with Acqis's counsel at Cooley to draft these materials but you reviewed them and signed them as your statement, correct? 09:15:24 09:15:27 09:15:30 09:15:34

A. Well, I mean the message in here, this is from -- is mine, right? And they helped, of course, to do a lot of the detail work, for example make sure all the references are right. 09:15:35 09:15:38 09:15:47 09:15:51

Q. And were you compensated for your time in connection with these two proceedings? 09:16:01 09:16:03

A. Yes. 09:16:07

Q. Okay. And what is the hourly rate at which you were being compensated? 09:16:07 09:16:09

A. €250. 09:16:11

Q. Per hour, correct? 09:16:13
A. Yeah. 09:16:17
Q. How many hours have you spent since your engagement to date on this effort? 09:16:18 09:16:23
A. I would have to look up my records, I don't remember the exact number. Altogether, up to date, 50 hours, maybe 60, let's say, plus or minus 10, 20 percent. If you want the exact number I would have to check my records. 09:16:28 09:16:32 09:16:35 09:16:44 09:16:48 09:16:51
Q. Approximate is fine. 09:16:53
Do you recall how much time you worked on each of the two different declarations? Roughly 50/50? 09:16:59 09:17:01 09:17:05
A. That I can't tell. A lot of material is relevant for both and, as you noticed, there is quite a bit of similarity between these two documents, so it is hard to say how to break this up between the two. 09:17:08 09:17:12 09:17:17 09:17:19 09:17:23
Q. And what did you do to prepare for your deposition today? 09:17:28 09:17:34
A. You mean after submitting these documents? 09:17:38 09:17:39
Q. Correct. 09:17:40
A. I read them several times again to 09:17:44

refresh my memory. I read the patents, the prior arts not every page, there's a lot of material. And I had a few discussions with Cooley to tell me how this is working because this is obviously different from a normal conversation. 09:17:47 09:17:55 09:17:59 09:18:07 09:18:11

Q. And how many times did you meet with counsel for Cooley to prepare for your deposition? So just the conversations you had with them relating to preparing for today. And I don't want to know the substance, you know, I just want to know how many times. 09:18:14 09:18:19 09:18:21 09:18:25 09:18:31 09:18:33

A. Now, I didn't really try to keep track of this particular element, so I have to rethink this and this will not be a very accurate answer. Three, four times. 09:18:40 09:18:42 09:18:44 09:18:48

Q. Well, those three or four times were some of them on the telephone and were some of them in person or were they all in person? 09:18:52 09:18:57 09:19:00

A. When we are getting close, in person. 09:19:02 09:19:03

Q. And in total how many hours would you say you spent to prepare for the deposition over the course of those three or four meetings? Estimates are fine. 09:19:04 09:19:07 09:19:10 09:19:19

A. Fifteen. Maybe 20, maybe less. I 09:19:21

mean that relates now to the question of the 09:19:24
total amount of time I spent and the more 09:19:27
detailed numbers you try to make me give, the 09:19:30
more the sum will possibly not match because all 09:19:32
the errors will become larger and larger. 09:19:36

Q. In your declarations you 09:19:41
identified material that you considered, starting 09:19:44
-- I mean in both of the declarations 09:19:49
approximately it's on page 5. Well, 3, 4 and 5. 09:19:52

Since you submitted these declarations, 09:20:01
in the course of preparing for your deposition, 09:20:03
did you review any additional materials beyond 09:20:06
what's listed? 09:20:09

A. At this moment nothing comes to my 09:20:13
mind. I don't think so. 09:20:15

Q. Did you have any communications 09:20:19
with anybody? After the declarations were 09:20:21
submitted but before your deposition, did you 09:20:27
have any communications with anybody other than 09:20:29
counsel to prepare for your deposition? 09:20:30

A. No, I don't think so. I don't 09:20:34
remember any. 09:20:37

Q. You never spoke to Dr. Chu, for 09:20:37
example, of Acqis? 09:20:41

A. No. 09:20:43

Q. You didn't speak to any of your colleagues associated with what's called the Bogaerts reference? 09:20:43 09:20:44 09:20:46
A. After the submission I did not, and I believe we have a non-disclosure agreement with Cooley so I even can't do that, right? I mean this proceeding is confidential, I can't talk to anybody. This whole context. 09:20:49 09:20:50 09:20:55 09:21:00 09:21:04
Q. All right, but you didn't talk to anybody? 09:21:06 09:21:07
A. (The witness shook his head.) 09:21:10
Q. Did you also review the Patent Owner Response filed by Acqis that was submitted to the Patent and Trademark Office at the same time at your declarations? 09:21:17 09:21:21 09:21:25 09:21:28
A. I have read that, both responses for both patents and -- yeah. 09:21:30 09:21:32
Q. Did you review them before they were submitted to the Patent and Trademark Office? 09:21:36 09:21:38 09:21:40
A. I'm not quite sure. I may have seen an early version. I'm quite sure I have not seen the final version and if so it was very late anyway. 09:21:46 09:21:50 09:21:53 09:21:59
Q. You are aware that those Patent 09:22:02

Owner Responses cite to your declarations, correct? 09:22:04 09:22:08
A. Yeah. 09:22:09
Q. And did you believe when you reviewed the Patent Owner's Response that the citations to your declaration were fair representations of your declarations? 09:22:10 09:22:14 09:22:18 09:22:21
A. Yes, I believe so. 09:22:24
Q. Okay. Was there anything in the Patent Owner's Responses that you didn't agree with? 09:22:26 09:22:31 09:22:33
A. I don't remember anything at this point. 09:22:33 09:22:35
Q. In preparing your declarations, outside of attorneys for Cooley -- just so I've got a clear record, I'm not sure if I got a clear record, it was my fault -- in preparing the declarations, other than counsel for Cooley, did you speak to anybody else to gain facts or information to help you make your declaration in this case? 09:22:35 09:22:44 09:22:47 09:22:49 09:22:52 09:22:54 09:22:58 09:23:00
A. I only contacted one person in this context and that is Hans Müller who is co-author on the RD24, on the, as you call it, Bogaerts reference about his recollection of the 09:23:07 09:23:09 09:23:17 09:23:20

public dissemination of that document. That was all. 09:23:26 09:23:29

Q. Did you mention that you spoke to Dr. -- is it Dr. Müller or is he mister? 09:23:29 09:23:31

A. Doctor. 09:23:35

Q. Doctor. Did you mention that you'd spoken to Dr. Müller in your declaration? I didn't see it. 09:23:36 09:23:37 09:23:43

A. I believe not. I tried to get something concrete from him, I didn't, so there wasn't any point mentioning it. 09:23:44 09:23:48 09:23:51

Q. What did you try to get that was concrete from him? 09:23:53 09:23:54

A. Whether he remembered the exact date when it was put on to the CERN internet so that it was accessible to everybody. 09:23:56 09:23:58 09:24:04

Q. He could not remember? 09:24:07

A. No. 09:24:10

Q. And he didn't have any information that he provided to you that would say one way or the other when it was put on that server? 09:24:10 09:24:12 09:24:15

A. The message was, "It's almost 20 years ago, how could I remember?" And, I mean, I put forth in my declaration quite a bit of text, and maybe we should go through this, 09:24:22 09:24:24 09:24:28 09:24:33

what we can say, what we cannot say and so forth. This is what basically came out of that. 09:24:37 09:24:40

Q. One question about the materials you did consider. One of them, the item that's listed in both declarations is the 2012 Federal Circuit Bar Association Model Patent Jury Instructions. Do you recall why you looked at those? 09:24:43 09:24:52 09:24:55 09:24:59 09:25:02 09:25:04

A. In order to understand what principles are to be applied and I mean this is one of the reasons why I put all of this into this document to make clear what are the principles which we had used in the analysis in this declaration. 09:25:06 09:25:09 09:25:14 09:25:17 09:25:19 09:25:22

Q. You understand that these two Acqis patents are part of a large family of patents that is owned by Acqis; is that correct? Do you understand that? 09:25:24 09:25:28 09:25:31 09:25:34

A. Yes. 09:25:35

Q. You didn't list having reviewed any of the other patents or patent file histories; is that correct? 09:25:35 09:25:40 09:25:43

A. Well, the list is quite long, we would have to go through this but if you say so I believe you. 09:25:45 09:25:46 09:25:48

Q. Do you know why you didn't look at 09:25:53
any materials from any of the related patents or 09:25:55
file histories? 09:25:59
A. I mean I was asked to form 09:26:00
an opinion about the case raised against these 09:26:04
two patents, whether or not they are valid or not 09:26:08
valid and this is what I did. And for my 09:26:11
analysis I used everything which I thought was 09:26:15
relevant and this didn't seem to be relevant in 09:26:18
order to also limit the amount of time which went 09:26:26
into this. 09:26:29
Q. For both declarations I noticed 09:26:33
that you did not provide a copy of your CV; is 09:26:37
that correct? 09:26:37
A. There is a short version of it in 09:26:43
here under Section II, for instance, in the 09:26:54
Document 01462, this is the '873 Patent, 09:26:56
professional qualifications, and there is 09:27:05
a similar one in the other one, which basically 09:27:07
says most of the things which I've done. It's a 09:27:11
high-level CV, if you want more details -- it's 09:27:15
relatively long -- you can have them. But we did 09:27:18
not include what is usually done like the most 09:27:22
important publications, patents filed and stuff 09:27:25
like that, because it didn't appear to be 09:27:28

relevant. 09:27:29
Q. Okay. I just wanted to confirm 09:27:30
that your CV was not attached as an exhibit and 09:27:34
what we have for your professional qualifications 09:27:36
in each proceeding is what you've provided in 09:27:39
Section II of your declaration; is that fair? 09:27:43
A. Yeah. Is there anything more you 09:27:46
like to know? 09:27:48
Q. No, I just trying to make clear 09:27:49
for the record what we have and what we don't 09:27:51
have at this point. 09:27:54
So in 1998 you had already received your 09:27:58
PhD in nuclear physics from Frankfurt University; 09:28:03
is that correct? 09:28:03
A. Yes. That was in 1993. I 09:28:10
graduated in 1993 and right after that I moved to 09:28:13
Lawrence Berkeley National Laboratory as 09:28:18
a so-called post-doc. I got a Humboldt 09:28:21
Fellowship, which is an award which basically 09:28:24
says, "Here's a bunch of money, do what you want 09:28:27
with it", it's quite nice. And although I have 09:28:29
a PhD in nuclear physics, I have the Humboldt 09:28:35
Fellowship in computer science, which is 09:28:40
untypical. I had a dual interest all my life and 09:28:43
my thesis is also -- it is nuclear physics, but 09:28:48

for it to be done it needed a quite big and 09:28:53
distributed computer to be built and it was 09:28:56
built, it worked, and with that working computer, 09:28:59
the data was recorded and that data was then 09:29:01
analyzed and for the analyzed data I got the 09:29:05
physics degree. And I did a Rigorosum, which 09:29:07
means there were three exams, one hour each, 09:29:14
theoretical physics, experimental physics and 09:29:20
computer science, which all had to be passed. 09:29:23
Q. Much of that answer is helpful but 09:29:37
I was just trying to get to a simple point. So, 09:29:39
by 1998, you had your PhD in nuclear physics from 09:29:42
Frankfurt University which you'd received in 09:29:46
1993; is that correct? 09:29:49
A. That is correct. 09:29:50
Q. And nuclear physics is the study 09:29:51
of what exactly, at a very high level? 09:29:54
A. This kind of instruction is not 09:29:57
ease. But Goethe used to say to understand what 09:30:07
keeps things together at its most fundamental 09:30:12
level. So nuclear physics tries to understand 09:30:15
the fundamental forces of nature of which there 09:30:21
are four but normal people only experience two, 09:30:22
gravitation and electric force, try to understand 09:30:29
what happens inside a nucleus. In our case we 09:30:36

tried to understand what happens at the Big Bang and why do we exist, rather fundamental questions. The principle behind that is all these experiments are rather large systems, we're talking at that time already millions of sensors read out at megahertz rate and that means no ordinary storage media could take such data and that requires a large amount of computer infrastructure to be in place so absorb that data and analyze that data. And that is one of the reasons why I chose that field because I had an area which really, really required the most cutting-edge computer infrastructure, computer architectures to do the job. Nothing could be purchased off the shelf. Sloppy spoken, it's a nice playground for somebody who's really interested in computer science. 09:30:40 09:30:42 09:30:46 09:30:51 09:30:57 09:31:02 09:31:07 09:31:11 09:31:14 09:31:18 09:31:22 09:31:24 09:31:27 09:31:32 09:31:34 09:31:41 09:31:44

My reason for answering your other question in a longer form was since you're emphasizing the PhD in nuclear physics, it might seem that I'm not an expert in computer science and this is why I tried to make that clear. And, as you see, although I have a PhD in nuclear physics, the next thing that happened was I was offered a chair in computer science, which is not 09:31:46 09:31:50 09:31:53 09:31:56 09:31:58 09:32:01 09:32:04 09:32:06

very usual. 09:32:10

Q. Okay, just to confirm, you do not 09:32:12
have a degree in computer science, correct? Your 09:32:15
degree is in nuclear physics even though you've 09:32:17
studied computer science? 09:32:21

A. I'm full Professor, endowed full 09:32:22
Professor in computer science, so ... 09:32:25

Q. But your degree is not in computer 09:32:27
science; is that right? 09:32:30

A. The PhD degree, yes. 09:32:31

Q. Well your undergraduate degrees 09:32:32
were not in computer science either were they? 09:32:35

A. The undergraduate degree is 09:32:39
physics, too. It's solid state physics, it's 09:32:39
about scanning tunneling microscopy, but it may 09:32:42
be surprising to you the scanning tunneling 09:32:48
microscope needed a computer to record the data 09:32:52
and an image analysis system to recalculate the 09:32:52
highly noisy signals which were recorded and I 09:32:56
built that system. So, again, I coupled computer 09:33:00
engineering/computer science with the 09:33:03
requirements in physics. It is always nicer to 09:33:06
build something which somebody needs than like 09:33:11
often happens some theoretical work is being done 09:33:16
but nobody has a real application for using it. 09:33:19

Relevance. 09:33:24

Q. Okay. But you mentioned computer 09:33:25
engineering, also you did not get a degree in 09:33:28
computer engineering what you're saying is you 09:33:35
took courses and studied that as part of the work 09:33:36
that you were doing in the physics field, 09:33:39
correct? 09:33:42

A. Yes, most of it is self-trained. 09:33:43

Q. Good. So then in paragraph 15 -- 09:33:45
and most of my questions are based on the '814 09:33:52
declaration, so the paragraph numbers might get 09:33:58
off if we use something else -- so the '814 09:34:00
declaration, paragraph 15, you offer your view of 09:34:03
what a person of skill in the art is for that 09:34:11
patent. Do you see that? 09:34:13

A. I pulled it up, yes. 09:34:15

Q. And a concept of a person of skill 09:34:15
in the art is based on your understanding 09:34:17
provided by counsel about what that means in the 09:34:21
patent law; is that correct. In paragraph 13, 09:34:24
for example, you explain what you understand a 09:34:28
person of skill in the art to be? 09:34:32

A. Let me look at it real quickly. 09:34:35

Q. Sure. And to be fair, 09:34:37
paragraph 14 also then explains what you 09:34:48

understand to be the appropriate level of the skill in the art, so I don't want to leave that one out. So it's 13, 14 and 15 sort of together. 09:34:50 09:34:53 09:34:55

A. Yes. Bachelor's degree, with a bit of focus on computer architecture, yes. 09:34:58 09:35:01

Q. And why did you choose bachelor's degree in computer science for the '814 Patent as opposed to other fields like physics or computer engineering? 09:35:06 09:35:12 09:35:16 09:35:19

A. Kind of obvious. This patent family relates to computer architecture. Although I should say it relates to parallel computer architecture and my understanding is, and that was confirmed by Cooley and I also believe I have read that in the declaration by Young, that this is the kind of level which is typically being used. So, you know, it can't be too high a level. It has to be an ordinary skill in the art type thing and that is what I understand has been considered as the typical level. 09:35:21 09:35:24 09:35:27 09:35:30 09:35:33 09:35:36 09:35:39 09:35:42 09:35:46 09:35:53 09:35:56 09:35:59

Q. Okay. It says in the middle, the person would hold a bachelor's degree or the equivalent in computer science or related academic field. What's your understanding of 09:36:00 09:36:06 09:36:09 09:36:13

what "related academic field" is? 09:36:15

A. This area, particularly when it is about computer architecture, has quite a few ties to engineering and computer engineering and you see that in particular since many of the schools in the U.S. even call themselves CSE/EE, Berkeley is an example, computer science/computer engineering. So that would be one example for a related field. But the fundamental knowledge which is required has a very -- has a strong element of computer science, right? I mean you have to understand how a computer works, how the different bits and pieces interrelate to each other, what are the appropriate standards in there being used, what are the principles to be used for what works, what doesn't work. And this is usually -- this is taught in computer science. If it then goes into how does it work in detail, how can it work, fast signals, slow signals, these kind of things, then engineering comes more and more into play. 09:36:19 09:36:24 09:36:29 09:36:34 09:36:38 09:36:45 09:36:47 09:36:49 09:36:56 09:37:00 09:37:02 09:37:05 09:37:10 09:37:11 09:37:13 09:37:16 09:37:21 09:37:24 09:37:27 09:37:31

Q. And what did you mean by "modular computing systems" in that definition? 09:37:35 09:37:41

A. Let me just check where is it? 09:37:48

Q. Two lines down where we were 09:37:51

looking:

"... and three to four years of additional experience in the field of modular computer systems ..." 09:37:52 09:37:53 09:37:57 09:38:03

A. Yes, I see. Many of the references which are being discussed here include systems which consist of different subfunctions, subsystems. Later they are being called or have been called nodes. So one computer, another computer, a network in between maybe a mass storage system somewhere elsewhere. In particular ... 09:38:05 09:38:11 09:38:16 09:38:22 09:38:27 09:38:30 09:38:34 09:38:34

(The court reporter sought clarification.) 09:38:34 09:38:34

THE WITNESS: Mass storage system. 09:38:34

And their interconnect matrix allows them to be combined in many different ways, and that means you have a modular system allowing different combinations of things together. And this is relatively different as compared to monolithic systems where, for instance, one example could be the Blue Gene family of computers which basically come as one big system where if you look carefully you still find the same building blocks, but they are all engineered 09:38:52 09:38:56 09:38:58 09:39:02 09:39:05 09:39:11 09:39:15 09:39:24 09:39:27 09:39:29

together as one thing and there is no interchangeability except you buy more nodes from the very same thing from the same vendor.

BY MR. BUROKER:

Q. Okay. Is it correct to say that by 1998 there were a variety of modular computing systems, computer architectures and computer communication protocols that were known to the person of skill in the art?

MR. DAVIS: Objection; form.

THE WITNESS: In order to give a very correct answer, the term "known" would have to be differentiated. Known in the sense of aware of existing certainly, yes. Known in the sense of being an in-depth expert is a different thing. This is why I hesitated to respond too quickly. Although we say here bachelor in computer science, the normal -- and I reviewed quite a few of the curriculum and I'm teaching this since 1998 in fact, in regular classes -- bachelor of computer science usually includes quite a bit of mathematics, learning to start programming. One has to understand where they come from, right, they come from high school and usually they have no knowledge, no concept of real programming,

except if you have a few geeks who did this by 09:41:15
themselves, like I did for example. But they 09:41:17
have to learn all of that, and then they learn 09:41:19
computer architecture but only computer 09:41:23
architecture in the sense of the single computer 09:41:25
with -- like one system. The entire context of 09:41:30
parallel systems with all the additional 09:41:36
complications which come in -- and I'm sure we 09:41:39
will get to that point later -- are not typically 09:41:42
part of the generic computer science curriculum. 09:41:46
So if you say "are known" the answer would be 09:41:52
they certainly knew it existed and they certainly 09:41:55
may have known the relevant particular buzzwords, 09:41:59
but the in-depth knowledge to know how a system 09:42:03
really works, to put such a system together, 09:42:06
debug it, find error, I would say likely not. 09:42:09
BY MR. BUROKER: 09:42:13
Q. Well, this person that we've 09:42:13
defined isn't just a beginning computer science 09:42:14
student, it's a person who's already received 09:42:21
their degree and worked for three to four years 09:42:23
in the field. So would that person have more 09:42:25
in-depth knowledge of modular computer systems, 09:42:27
computer architecture and communication 09:42:32
protocols? 09:42:33

MR. DAVIS: Objection; form. 09:42:33
THE WITNESS: Whether generic 09:42:38
experience working in the field at this abstract 09:42:40
level, the answer would be no. There would have 09:42:45
been some additional teaching and specialization 09:42:47
have to happen after the degree as a bachelor. 09:42:51
And maybe I should clarify that. I 09:43:01
mean I do teach a class about parallel computer 09:43:05
architecture since many years now, and this is 09:43:08
going a full semester, it's a full big class with 09:43:10
everything, and it is far not enough to get the 09:43:14
relevant knowledge into the heads of the students 09:43:21
and this is master level. 09:43:23
BY MR. BUROKER: 09:43:23
Q. In what year did you begin working 09:43:30
on modular computer systems, computer 09:43:33
architecture and computer communication 09:43:39
protocols? That was well before '93 I assume. 09:43:44
A. It's not possible to give an exact 09:43:47
and good date but in order to give you an answer 09:43:55
maybe I just tell you what I did and then you see 09:44:00
how things evolved. At the age of -- 09:44:02
Q. Well, I'm asking for a very 09:44:06
specific -- I know that you like to answer 09:44:07
questions in your way and you're welcome to, I'm 09:44:10

asking for a year. So, if you can answer that 09:44:12
question then I'm happy to have you give 09:44:15
an explanation. 09:44:18

A. My first modular and own computer 09:44:18
I got and improved and built was at the age of 09:44:24
probably 17. Now, I have to calculate the year. 09:44:28
You know my age so, I'm 52 years old, so at the 09:44:34
age of 16, this is 36 years ago, right? 2015 09:44:41
minus 36 we're talking something like 1980. That 09:44:53
was a Z80 computer, 8-bit machine. Then I later 09:44:57
started connecting multiple of those, building 09:45:02
larger systems all by myself. I financed my 09:45:06
studies by building computers for industry and 09:45:09
they paid me for it, which shows this is going 09:45:12
back quite some way. I already outlined doing my 09:45:17
diploma pieces I built such a system from 09:45:23
scratch. In the thesis it was a larger system 09:45:26
and, in fact, it is the first bigger highly 09:45:28
modular interconnected system I believe that was 09:45:33
ever built, and this is timescale '93. So it's 09:45:36
going back a long time. 09:45:40

Q. So, would you consider yourself to 09:45:44
be an expert in the field of modular computing 09:45:46
systems, computer architecture and computer 09:45:50
communication protocols? 09:45:53

A. Yes. 09:45:54
Q. Okay. So when you're doing your 09:45:54
analysis in connection with this case and 09:45:57
providing this declaration, were you looking at 09:45:59
things from your perspective as an expert, or 09:46:03
from the perspective of a person of skill in it 09:46:07
the art as you've defined it, which is someone of 09:46:08
less experience than you? 09:46:13
A. Had to be, yes. And I believe I 09:46:16
set this forth, I mean the definition of a person 09:46:18
of ordinary skill in the art is set forth in the 09:46:21
declaration, and my understanding is this is the 09:46:24
perspective which had to be used. 09:46:29
Q. Right. So you used the 09:46:34
person-of-skill-in-the-art perspective as opposed 09:46:36
to your own, correct? 09:46:38
A. Does it have to be opposed to? 09:46:42
Q. Well, in analyzing the opinions, 09:46:46
whether something is obvious or anticipated or 09:46:50
known, did you do that from the perspective of 09:46:53
a person of skill in the art or from an expert's 09:46:56
perspective? 09:47:01
A. Now I understand the subject 09:47:07
material of course as an expert. The conclusions 09:47:08
drawn in here I believe are valid in both cases, 09:47:12

and we can go into details, but in principle they 09:47:17
would have to be -- would be taken in the view of 09:47:22
the person of ordinary skill in the art because 09:47:25
this is how it works. 09:47:28

Q. So what I've handed you is what we 09:48:58
call the Bogaerts reference which is Exhibit 1011 09:49:01
in the 1469 IPR proceeding which is the one 09:49:08
related to the '814 Patent. Make sure I have the 09:49:14
numbers right, there are a lot of complicated 09:49:25
numbers here. 09:49:27

So, are you familiar with this document? 09:49:28

A. Yes, I am. 09:49:30

Q. Okay. And, in fact, if you look 09:49:31
at -- I'm going to have you do two things at once 09:49:34
-- paragraph 170 of the '814 declaration which 09:49:40
you were just looking at, the first sentence 09:49:44
says: 09:49:48

"I am an author of the Bogaerts 09:49:49
reference." 09:49:52

Is that correct? 09:49:52

A. Yes, as you can see on the front 09:49:53
page. 09:49:55

Q. In other places I think you also 09:49:55
say you're a co-author but you basically mean 09:49:57
you're one of the authors, correct? 09:50:00

A. Yeah. There is only a very minor distinction between the two and that is more a game played in research of who is called the primary or first author and who is called the last author and that even is different in the different fields. So in medicine the last author is always the group leader. Here this is a status report and basically there is just basically a list of those who have contributed.

Q. That's what I wanted to get to. Was there a primary author of this status report?

A. The way it worked was this is a status report of a working group, this RD24, which was chaired by Hans Müller and he did the writing most of the time, putting things together where everybody delivered bits and pieces. So I certainly delivered also some chapters here, in particular about the PCI-SCI bridge. Then it was circulated and at some point everybody said it's okay to be our status report at this particular time.

Q. Did everyone on the front page of this document contribute to the text of the status report?

A. I certainly did. I can't tell for

everyone in particular because, you know, I haven't checked every email which went possibly directly to Hans Müller, but certainly everybody was involved here. I know most of the people personally, actually I know all of them pretty much, although many have disappeared from this research field. 09:51:35 09:51:38 09:51:42 09:51:46 09:51:50 09:51:54 09:51:59

Q. So how was this document compiled? You mentioned emails. How did it get to be in the form that it's in? 09:51:59 09:52:01 09:52:05

A. I remember Hans Müller likes to write with FrameMaker, which is a text writing tool, I'm not sure it exists anymore, quite a nice thing. I believe at that time I had FrameMaker, too. And the important thing was are the results we can present which are convincing, showing that there was great progress? These results were pulled together, sent forth and back. I mean you have to understand I was in Berkeley, California, this is nine hours' time difference. I spent frequent time at CERN at that time going constantly forth and back. 09:52:10 09:52:13 09:52:17 09:52:21 09:52:26 09:52:33 09:52:36 09:52:40 09:52:45 09:52:48 09:52:49 09:52:52

Andreas Bogaerts is CERN. 09:52:57

We have the University of Oslo, Bernard Skaai he's retired now. Oslo is a two- or 09:53:00 09:53:03

three-hour flight from Geneva, so for them it was also quite an effort to get there, they did a lot of their work at Oslo.

Spain. We had a student who worked at CERN but the group leader was in Spain so, again, requirement for interchange.

Kare Løchsen and Hugo Kohmann is Dolphin, again same thing. Dolphin's role was the supplier of many of the chips which are being discussed in here and being evaluated, tested and so forth, being part of a ...

Digital Equipment is head of joint project with CERN and I believe this is the Geneva branch of Digital so he was close. He could have had direct interactions with Hans Müller.

Q. Right, so the question that I asked was more, you know, was there a person who typed in all the text or did each of the various people send sections to be posted into the document? How was it compiled?

A. Both. I mean this is almost 20 years ago.

Q. Right.

A. But this was nothing out of the

ordinary, and the normal way it goes is people send in stuff, text blocks, figures, diagrams. I'm quite sure this diagram is from myself. The big picture I believe Hans Müller did, although the board I believe is the one I supplied. You know, these kind of details. And then Hans Müller put it together in a big document, then we went over it, and at some point it was the final version, a postscript file was generated and this is what was submitted. 09:54:24 09:54:27 09:54:32 09:54:35 09:54:38 09:54:42 09:54:46 09:54:48 09:54:50 09:54:54

Q. So based on your recollection, which portions of this document did you write or which figures did you contribute? 09:54:55 09:55:00 09:55:03

MR. DAVIS: Objection; form. 09:55:07

THE WITNESS: I mean, this is really a long time ago. My focus of work at that time was the PCI-SCI adapter, which you may have noticed is a core device in this whole document, because many of the system architectures which are sketched and outlined here need this as a fundamental building block. And I was basically working with very a significant fraction of my time on this device because I needed it for myself in Berkeley. We were trying to build a very large data acquisition system and 09:55:14 09:55:17 09:55:25 09:55:29 09:55:32 09:55:36 09:55:39 09:55:43 09:55:47 09:55:49 09:55:52

we needed the PCI-SCI device for that. So that means Section 3.1 is a very strong candidate for me being involved. You also see that there is a small -- 3.2 says, "Collaboration ... with the STAR Trigger group", which is me basically. STAR is the name of an experiment being prepared at that time at Brookhaven National Laboratory. STAR stands for solenoidal tracker at RHIC. S-o-l-e-n-o-i-d-a-l tracker at RHIC. A solenoid is a particular kind of a magnet. 09:55:55 09:55:58 09:56:06 09:56:11 09:56:15 09:56:21 09:56:23 09:56:28 09:56:34 09:56:43

BY MR. BUROKER: 09:56:50

Q. So, at least -- and there may be others -- but you recall at least contributing to 3.1 and 3.2? 09:56:50 09:56:52 09:56:58

A. These would be the core ones. I have been involved in other stuff. I have certainly read it and looked at it, but I can't remember the details after such a long time. 09:56:59 09:57:01 09:57:03 09:57:11

Q. This document talks about two different PCI-SCI adapters, correct? There's the CERN one which you mentioned and then there's also one by Dolphin; is that right? 09:57:15 09:57:22 09:57:26 09:57:28

A. Correct. 09:57:31

Q. Did you work on the Dolphin PCI-SCI adapter? 09:57:31 09:57:33

A. No. I believe at that time it didn't really fully exist yet. Let me just check. Do you remember which section it is being discussed? Here we are. 09:57:35 09:57:39 09:57:45 09:57:49

Q. Where are you looking? 09:57:59

A. Section 3.3, it says: 09:58:00

"RD24 has acquired Dolphin bridges ..." 09:58:03

Not sure it existed yet or what state it was at that time. 09:58:23 09:58:25

Q. Okay. How did you come to be involved in this RD24 project? 09:58:31 09:58:47

A. I need to outline what this is all about in order to make this clear. 09:58:55 09:58:58

"RD" stands for "research and development" and 24 simply means it's the 24th research and development project at CERN. This nuclear physics or high-energy physics field has a particular problem. It takes some often 25 years to prepare an experiment, this long, and at the LHC we're talking about that kind of time. The LHC was first started to be planned around 1980, the first proposals, the first documents, how it was going to be were written at that time, and it went in operation 2007/8/9, I can't remember exactly. 2005 it was scheduled but 09:59:00 09:59:02 09:59:06 09:59:11 09:59:15 09:59:21 09:59:25 09:59:30 09:59:33 09:59:36 09:59:39 09:59:47

there were delays. And when it was started, 09:59:49
there were many areas where the proposal 09:59:54
basically said today no known technologies exist 09:59:58
to solve the problem, in particular in computer 10:00:01
engineering areas. Everybody likes to refer to 10:00:05
Moore's law like things will get faster and 10:00:08
cheaper but, of course, over a period of 25 years 10:00:13
we're talking at the least three, four computer 10:00:15
generations, it is rather difficult to make 10:00:19
a clear, dependable proposal that how it would be 10:00:21
to build such a system and how much it would cost 10:00:24
because when you submit a proposal you have to 10:00:27
have a cost figure. So in order to avoid either 10:00:29
using hopelessly dated technology when the 10:00:34
experiment went online -- and, I mean, the LHC 10:00:37
project all together is a $6 billion project, 10:00:40
it's not a cheap thing -- there had to be 10:00:43
research and development done in order to 10:00:47
minimize the risk of uncertainty which technology 10:00:53
to use and that the technology would still be 10:00:55
available when the experiment and the accelerator 10:00:57
would go online. Lots of technologies come and 10:01:01
go. And RD24 is the research and development 10:01:03
project which was set forth to investigate and 10:01:08
develop a modular, highly scaleable computer 10:01:11

architecture, scaling to literally thousands of 10:01:14
computer nodes. The CERN experiments today have 10:01:17
thousands of computers connected together to 10:01:20
process the data of each and every experiment 10:01:23
there, huge effort, it would fill the entire 10:01:25
building, yeah? And there was no network 10:01:30
existing which would solve these problems, so 10:01:34
RD24 decided to focus on SCI -- the scalable 10:01:40
coherent interface -- as a very good and strong 10:01:44
candidate for solving these problems. So this is 10:01:46
the context. 10:01:49

I was working at that time in Berkeley, 10:01:50
for the STAR experiment at the Relativistic Heavy 10:01:53
Ion Collider in Brookhaven. 10:02:06

(The court reporter sought 10:02:06
clarification.) 10:02:06

THE WITNESS: Relativistic Heavy Iron 10:02:08
Collider. Relativistic stands for that the 10:02:10
particles basically have speed of light. And 10:02:11
same problem, long-term development, yet 10:02:15
requirement to make clear proposals how one could 10:02:21
actually handle this kind of amount of data. 10:02:25

When I started in Berkeley, I was asked 10:02:28
to do a technology evaluation to look at ATM, at 10:02:32
fibre channel -- f-i-b-r-e channel the English 10:02:38

spelling, the technology uses that -- and SCI. 10:02:43
I discarded ATM for making no sense, I 10:02:48
didn't like fibre channel, and focused on SCI. 10:02:52
So it was obvious that we work together with the 10:02:55
people doing the same thing at CERN. The amount 10:02:57
of R&D which was necessary was just way too much 10:03:03
to be done by a small group all by itself. So, 10:03:07
we joined forces basically. 10:03:10
BY MR. BUROKER: 10:03:13
Q. Did you already know Dr. Müller 10:03:13
before you got involved or who was your point of 10:03:17
contact when you first got involved with the RD24 10:03:20
project? 10:03:25
A. I'm not 100 percent sure. The 10:03:30
problem is I am affiliated with CERN since I'm 10:03:32
a PhD student. CERN use technology I developed 10:03:38
while I was already at GSI and used it for the 10:03:41
CERN experiments. So I have a CERN user ID and I 10:03:43
could go there any time and I retained that when 10:03:47
I was in Berkeley. 10:03:50
My best guess is that Dave Gustafson, 10:03:53
the author and Chair of the SCI Committee, the 10:04:00
SCI standard -- who was indirectly involved in 10:04:04
this as well but he wasn't a member of the 10:04:07
working group and therefore is not author on this 10:04:09

document -- may have said, "Hey, do you know there is a group, wouldn't it make sense for you to be involved?" It may also be that I just -- that we already had something to do earlier. I would really have to check my records more than 20 years ago, I'm not sure I still have all the emails. But in this area, this is a highly specialized very high-tech, cutting-edge field, the community is small and they are usually -- and we had, too, certain kinds of conferences, working meetings and so forth, so it was almost clear that we had to bump into each other and then decide that it makes sense to work together. 10:04:11 10:04:13 10:04:16 10:04:25 10:04:28 10:04:30 10:04:32 10:04:38 10:04:45 10:04:51 10:04:53 10:04:58 10:05:00

Q. So you mentioned that you were helping to develop what you mentioned in the document as the CERN PCI-SCI adapters. Did any of the other people on this document help you with that? 10:05:05 10:05:07 10:05:10 10:05:14 10:05:16

A. The part of this document I don't like is the CERN PCI-SCI adapter because the majority of the work I have done myself. But, yes, there has been cooperation and I remember I spent something like close to two months at CERN, when we decided, "We are rather close, let's do some real push together", but I can't tell 10:05:23 10:05:26 10:05:30 10:05:33 10:05:37 10:05:41 10:05:46

whether this was before or after the submission of this report because if you know -- you may have noticed but this report states rather clearly that this device was not finished at all at that time, and we can get to the details. I remember working with Bin Wu -- B. Wu -- he's a Chinese person. At that time I believe he was post-doc. I believe also one of Valencia students who were there at the time, I remember we were a group of three people basically working together, but since the other names I don't think were directly involved in this particular case, and we're talking real hard-core engineering development of gates, writing the HDL codes, synthesizing, time enclosure kind of thing.

Q. Did you all have -- strike that.

As part of the RD24 project were there regular conference calls or meetings?

A. Yes.

Q. Did you physically inspect the computer systems that other people in the project were working on?

A. Yes, many of them have been set up also for demonstration at CERN. This is one of those sad stories in research, the big labs have

the big money, the universities don't, so many of 10:07:35
those things were really expensive. So CERN had 10:07:38
the money to buy them and then all the 10:07:41
universities would basically go to CERN in order 10:07:45
to be able to play with them. I used, for 10:07:48
example, also the simulation framework developed 10:07:53
in Oslo to evaluate and extrapolate performance. 10:07:57
I believe the VME system was at CERN. 10:08:03

Q. When you say the "VME system", 10:08:08
which one are you referring to? The one in 10:08:11
Figure 15 or some other one? 10:08:14

A. The PCI-SCI card which I focused 10:08:23
on is -- if you look at Figure 4, you will see 10:08:26
this device which has a rectangular shape. And 10:08:31
it's called PMC 75 by 150 millimeters. "PMC" 10:08:38
stands for "PCI mezzanine card". It is not the 10:08:44
PCI form factor as set forth in the PCI 10:08:47
specification, PCI 2.1, which was the relevant 10:08:51
one at that time. There is an add-on spec which 10:08:55
says use everything as written in the PCI 2.1 10:09:00
spec except for the mechanical form factor, use 10:09:03
that form factor and these white connectors to 10:09:06
your right, such that you can plug them into 10:09:09
a VME board. Most VME processors use PCI also, 10:09:12
but in a different form factor because they 10:09:17

wouldn't otherwise fit into these crates. And so 10:09:20
then, for example -- now I'm trying to find this 10:09:24
picture, it's the VME module with a PMC on it. 10:09:29
And these evaluations were done. Yeah, for 10:09:36
example, Figure 19 you see the VME board and the 10:09:39
PMC card. 10:09:40

Q. I see. And you physically saw 10:09:50
this? What's shown in Figure 19, is a depiction 10:09:58
of something that was built and that you saw at 10:10:02
CERN? 10:10:05

A. In one or a different 10:10:07
incarnations. I mean this is a lab, right? 10:10:09
Things have been put together, taken apart, 10:10:12
reconnected, yeah, but this system or a variant 10:10:14
of that I've certainly seen. 10:10:19

Q. And as part of this project, how 10:10:24
frequently did you say you travelled to CERN? 10:10:27

A. I can't tell exactly, once or 10:10:42
twice a year, this kind of thing. You have to 10:10:44
remember I was in the U.S. first as a foreigner, 10:10:47
I came in on a J-1 visa. Then I changed to 10:10:51
an H-1, and then I got the green card based on 10:10:55
the national interest waiver. Before I had the 10:10:58
green card, leaving the U.S. was quite a painful 10:11:02
thing. So this was not just something you just 10:11:03

decide and do the next day. But even with this corollary I believe I certainly did one or two trips a year to keep the work going, there is only so much you can do over email and video conferences. 10:11:06 10:11:16 10:11:19 10:11:25 10:11:29

Q. In terms of this particular status report, that's Exhibit 1011, do you recall seeing a draft of it before it was submitted? 10:11:29 10:11:31 10:11:38

A. I assume so. I don't explicitly recall seeing a draft, this is too long a time ago, but the way this was usually done -- in fact, in the research field submitting a document with an author on it without the author seeing it beforehand would be an outrage, you can't do that really. But if you ask me, "Do you remember when you saw this?" this I cannot tell, this is too long ago. 10:11:42 10:11:45 10:11:48 10:11:53 10:11:58 10:12:01 10:12:04 10:12:07 10:12:10

Q. So standard protocol because your name is on it is that everybody on this particular document would have been provided a copy before it was submitted, correct? 10:12:10 10:12:12 10:12:15 10:12:16

A. Good conduct would be and everybody says, "Yes and I agree with the content in there." 10:12:19 10:12:21 10:12:22

Q. You say in your declaration that 10:12:24

it was submitted to somebody. Who was it submitted to that you recall?
A. LHCC Committee. I guess I should do some explanation here --
Q. Sorry, I apologize but --
A. LHCC.
Q. Okay, so there's also an LHC, what is the difference? What does "LHCC" stand for? Is that the LHC Committee?
A. More or less, yes, but I wish to give you a few more details because otherwise this is too broad a term and it doesn't come clear what this is all about.
Q. Okay, let me just for clarity ask you what does "LHCC" stand for then?
A. This a review committee which was put into place to monitor and evaluate the progress of all related research and development groups of the LHC project and all other projects all together. So, I have reported to the LHCC every three months since 1998 for stuff right outside RD24.
This is a very, very tough review process. So you submit a document, you then basically report orally. The committee then

writes a report and the report is then reported to the CERN Director and only the committee can defend your project, so you have to teach the reviewers that they defend your project in front of the CERN Director, Scientific Director. 10:13:50 10:13:54 10:13:59 10:14:02 10:14:05

So the idea behind it is that you have to be -- it's not just, you know, you thumb over some documents and say, "Well it's cool, it's all right", but a very stringent, very tough review process in order to make sure that this huge highly complex project has a chance of succeeding. 10:14:08 10:14:10 10:14:13 10:14:16 10:14:20 10:14:23 10:14:25

All these processes were following a rather strict order and an internal rule set. The reviewers were usually set out to accompany a particular project for a longer period of time, we're talking several years, and if the reviewers would say, "This project is not performing" rather tough scrutiny would happen. I've seen it happening -- fortunately never in my own case -- that you get down to weekly and even daily reports when you're really starting to get into bad shape. 10:14:27 10:14:31 10:14:37 10:14:40 10:14:43 10:14:49 10:14:53 10:14:57 10:15:00 10:15:04 10:15:08

The idea behind it is to have a complete view of this huge development -- the same was 10:15:09 10:15:11

done for the accelerator, for example -- to make sure that everything comes together in time. 10:15:14 10:15:16

Q. So I understand it, there are a number of different projects that were related to the LHC and this RD24 was one of those projects, correct? 10:15:18 10:15:21 10:15:23 10:15:30

A. Yes. 10:15:31

Q. And so the status report was a report created by the RD24 working group that was submitted to the LHCC as part of some periodic review? 10:15:31 10:15:33 10:15:38 10:15:42

A. Yeah. 10:15:43

Q. Okay. Who is on the LHCC at that time? In general, what kinds of people? 10:15:44 10:15:47

A. People my status. 10:15:52

Q. Okay. 10:15:53

A. Director of an institute, full professor, ten years' minimum experience in the field, highly outstanding scientific record, publication record. And, in fact, it was an issue over time -- because this is a huge amount of work for the reviewers, too -- to really find people at that level. We're talking around the globe, all time zones, they all had to travel to CERN, get together, do their work. 10:15:54 10:15:59 10:16:01 10:16:08 10:16:10 10:16:12 10:16:15 10:16:17 10:16:23

Such a review, the bigger ones which were quarterly, usually took a couple of days depending on the size of the project. Now, RD24 would be considered a small project, right? If you take the ALICE experiment, the ALICE experiment had some 20 subprojects, where each one was at least at large as RD24 and they all were reviewed like that, you know. 10:16:25 10:16:29 10:16:31 10:16:34 10:16:37 10:16:40 10:16:44 10:16:47

Q. So, how many people in this 1996-1998 timeframe sat on the LHCC? 10:16:49 10:16:54

A. I can't give you an exact number. We're talking a handful, three, four, five. Depending on the particular project being reviewed. In the case of ALICE the group was larger because the spread of different technologies was larger. Here this is -- in quotes -- only computer architecture, computer engineering. Normally you have detector physics on top of it, material science. Detectors are highly complex devices pushing the limits of material science, for example, so you have people understanding that also. 10:17:01 10:17:03 10:17:07 10:17:11 10:17:16 10:17:18 10:17:24 10:17:27 10:17:31 10:17:35 10:17:38 10:17:40

But the LHCC is a whole body all together, so it would all come together then and then be reported, all subprojects. It's a big 10:17:42 10:17:45 10:17:48

thing.

Q. So at the top of the document there's a heading in the right and it says: "CERN/LHCC" and then "LHCC 96-33". Do you know what that means?

A. I would assume this is the year and probably the 33rd kind of meeting of that. The exact number scheme I don't know. It's an internal LHCC coding so that they find their reports.

Q. Okay, and then it says "LCB Status Report". Do you know what "LCB" means?

A. I do, but now I don't remember the exact acronym. It could be LHC Computing Board, something like that.

Q. And the "2 October 1996", you indicate in your declaration that you believe that is the date that this status report was submitted to the LHCC; is that correct?

A. Yeah.

Q. And what is the basis for -- do you have any basis for that other than your memory for saying that that's the date it was submitted to the committee?

A. This is a status report of

10:17:51 10:17:52 10:17:57 10:18:01 10:18:10 10:18:13 10:18:15 10:18:19 10:18:24 10:18:27 10:18:27 10:18:32 10:18:37 10:18:41 10:18:49 10:18:53 10:18:58 10:19:00 10:19:02 10:19:05 10:19:05 10:19:12 10:19:15 10:19:17 10:19:20

a working group which is basically documenting a work in progress. Many things in here are outlined as options for the future or how one could do things, what are the things which are essential to be built, how far the process of building has come. And obviously that has to have a date as of when this status has been written and submitted because obviously if you report time in progress, the next day it's already invalid, strictly spoken, and this is the date when this was submitted. There is no other date on this document.

Q. Right so --

A. I have one question or favor to ask. I would like to go to the bathroom.

MR. BUROKER: Oh, yeah, I should have said at the beginning, any time you need to take a break, we can take a break. So let's go off the record and take a short break.

(Brief recess 10:20 a.m. - 10:27 a.m.)

BY MR. BUROKER:

Q. Sir, looking at paragraph 170 of the declaration we were looking at before in the '814 proceeding, you state that the date on the front of the Bogart reference, which is

Exhibit 1011 we were looking at, has a date and 10:28:05
that's the date submitted to the CERN LHCC 10:28:09
Committee. That's your testimony, correct? 10:28:14

A. Yeah. 10:28:15

Q. And you don't cite anything to 10:28:16
support that, that's just your testimony based on 10:28:19
your memory of how the proceedings were, correct? 10:28:25

MR. DAVIS: Objection; form. 10:28:31

BY MR. BUROKER: 10:28:32

Q. Right? Next to that sentence 10:28:33
there's no citation to any other document or 10:28:34
piece of evidence, just your memory, correct? 10:28:36

A. Well, I mean if you write 10:28:39
a document, a report of any sort, in particular 10:28:41
a status report, it is completely invalid without 10:28:46
a date. So this date has to be the date when 10:28:49
this report was finalized as the status of the 10:28:59
RD24 project at that time. If you would remove 10:29:04
that date, or declare it to be something else, 10:29:12
this status report would be meaningless. 10:29:15

Q. Right. But you're trying -- 10:29:17
strike that. 10:29:17

You're saying also that that date 10:29:23
represents the date submitted to committee and 10:29:25
not the date of its public availability or 10:29:28

indexing by the library. And for that proposition you also do not cite anything, correct?

MR. DAVIS: Objection; form.

THE WITNESS: This is the date which defines the status of that report and this is the date when it was submitted -- this is the date when it was given to the LHCC, possibly one or two days later. Usually they were written up to the last minute, you know, all these reports are usually generated, everybody's late. And from this document, or anything I've seen so far, I have not seen any evidence that says that it was then publicly available, that's correct.

BY MR. BUROKER:

Q. All right. But you also don't know, and can't provide testimony, that it wasn't publicly available as of October 2, 1996, right?

MR. DAVIS: Objection; form.

THE WITNESS: I mean here I wish really to stick to what I say in my report. What do we have here? I'm saying I'm unaware of any day prior to the priority filing date of the '814 Patent that the RD24 report was published, indexed or made available to the public, which

are the relevant things here. So this is what it is: I'm not aware. I'm not saying it was, I'm not saying it was not, I'm just not aware. 10:31:07 10:31:13 10:31:17

BY MR. BUROKER: 10:31:20

Q. Okay. In the previous sentence, you say -- strike that. Let me come back to that. 10:31:21 10:31:22 10:31:28

Then in paragraph 171 you make reference to: 10:31:29 10:31:37

"... bibliographic data on the CERN library server that lists the Bogaerts reference as 'submitted by October 2, 1996' ..." 10:31:43 10:31:46 10:31:50

And you say: 10:31:52

"[It] relates to the date the ... report was submitted to the ... committee; it does not relate to the day the RD24 report was available or indexed in the CERN library." 10:31:52 10:31:53 10:31:55 10:31:59

What's your basis for saying that? 10:32:02

A. Is there any date? I can't see any date on the CERN library stamp. I mean this is an index basically uniquely identifying this document as part of the CERN library, it says nothing about its public availability. And one should make one thing perfectly clear here, even if a document is in the CERN library, it's far 10:32:05 10:32:08 10:32:11 10:32:14 10:32:17 10:32:21 10:32:24

from being publicly available. In order to get to the CERN library you have to cross the CERN entry, and the CERN entry you can only cross if you're a CERN member. The United States are not member state of CERN. So, for instance, nobody from the U.S. could easily be entering CERN at all. You first have to become at least a guest of CERN, which means you have to have a project at CERN or with high relevance to CERN, like I did, but I had my ID already beforehand, and then you can go to the CERN library on site of CERN. Be aware, CERN is an international organization; when you enter CERN you basically leave Switzerland, right? It is a state in itself, and has very high standards with respect to its autonomy. So even if this document is in the CERN library, it doesn't say that it automatically is on the internet. There is a huge amount of documents in the CERN library which would also never make it to the internet because of all the copyright issues associated. 10:32:26 – 10:33:30

Q. But a document doesn't have to be on the internet to be a publication under U.S. patent law, correct? 10:33:38 – 10:33:45

A. Right. Now, if you're referring 10:33:46

to the -- there is a definition for public availability which I have put in here I believe. Do you want me to cite it? 10:33:49 10:33:53 10:33:58

Q. Well, if you need to to answer the question I asked which is that a document doesn't have to be on the internet to be considered a publication under U.S. patent law? 10:33:59 10:34:02 10:34:05 10:34:07

MR. DAVIS: Objection; form. 10:34:10

THE WITNESS: Let me just pull this out to be really precise. (The witness reviewed the document.) 10:34:14 10:34:15 10:34:15

Right: 10:34:27

"A reference must have been made, known, used, sold, offered for sale, published, or patented or be the subject of a patent application by another, before the priority date of the patent." 10:34:27 10:34:30 10:34:32 10:34:34 10:34:36

There is also a section which says the index is searchable so that it can be found. That section I have a problem finding at this moment. Ah, here we are, page 8, paragraph 19: 10:34:37 10:34:40 10:34:49 10:34:52

"I understand that a reference is considered publicly accessible if it was ... publicly disseminated or (2) otherwise made available to the extent that persons interested 10:35:00 10:35:01 10:35:04 10:35:08

and ordinarily skilled in the subject matter or art, exercising reasonable diligence, could locate it."

And, I mean, this is the sentence here, right? Because it was stored in a library doesn't mean it's publicly available and this is why I made this statement about the CERN library.

BY MR. BUROKER:

Q. Well the next sentence though you say you recognize that if it's in a library and it's indexed and cataloged by title or subject matter that's a factor that means it could be considered publicly accessible?

A. Provided the library has public access. If there is a library which is private, you can't get to, and there is no public access.

Q. Well that's not what it says in your declaration; you didn't say that the library has to be publicly accessible.

MR. DAVIS: Objection; form.

BY MR. BUROKER:

Q. Did you?

A. Can you ... where did I say that?

Q. Well that's my point. I don't believe you said -- the last part of your answer

in the previous question was "provided the 10:36:11
library has public access". I don't think that 10:36:14
any of this text in paragraph 19 says that the 10:36:16
library has to have public -- be accessible to 10:36:18
the public, does it? 10:36:22

MR. DAVIS: Objection; form. 10:36:24

THE WITNESS: Well, take paragraph 19, 10:36:30
second sentence: 10:36:32

"I understand that publicly accessible 10:36:32
requires that a reference must have been 10:36:36
sufficiently accessible to the public interested 10:36:38
in the art." 10:36:41

BY MR. BUROKER: 10:36:43

Q. Right, and one of the kinds of 10:36:44
people who would be interested in the art would 10:36:45
have been a person working on computer 10:36:47
architecture as part of some of the CERN 10:36:52
projects, right? 10:36:56

MR. DAVIS: Objection; form. 10:36:56

THE WITNESS: Not necessarily. 10:36:57

BY MR. BUROKER: 10:37:00

Q. Were you interested in the art? 10:37:01

A. Yes. 10:37:03

Q. And you could have accessed it, 10:37:03
correct? 10:37:04

A. I have a very particular history in this particular field, but this field is of course much broader and larger than just nuclear physics. 10:37:04 10:37:07 10:37:15 10:37:19

Q. Well, anybody on this RD24 status report, any of these people would have had access to the CERN library in 1996, correct? 10:37:19 10:37:21 10:37:23

A. Absolutely, yes. 10:37:25

Q. Among other people working on various LHC projects? 10:37:26 10:37:28

A. Correct. Basically all CERN users. 10:37:31 10:37:38

Q. You agree that this document was at some point provided to the CERN library, right? 10:37:40 10:37:45 10:37:48

A. Correct. Otherwise there wouldn't be the library stamp on it. 10:37:50 10:37:51

Q. Okay. Do you have any knowledge regarding the procedure by which this document was provided to the CERN library? 10:37:53 10:38:01 10:38:04

A. I would assume it's the normal procedure, submission to the library, library records it, puts the stamp on it. Other than that no, and I was not involved when this happened. 10:38:08 10:38:10 10:38:14 10:38:17 10:38:20

Q. Did you ask Dr. Müller if he submitted it to the library? 10:38:20 10:38:27

A. I asked him whether he had a recollection when it was done and he said no. I didn't ask him explicitly, "Did you do this?" but I believe that one can assume that he did. 10:38:28 10:38:30 10:38:32 10:38:35

Q. So it's possible that he submitted it to the library at the same time that he submitted it to the CERN LHCC Committee, correct? 10:38:39 10:38:40 10:38:43

A. I don't know that. 10:38:49

Q. It's possible and also not possible, right? 10:38:51 10:38:54

MR. DAVIS: Objection; form. 10:38:59

THE WITNESS: I mean, in general, keep in mind the frame setting of this here, this is a tough review committee, you're reporting to such a review committee. I would never, ever submit an internal document I give to a reviewer, in particular if it contains some confidential information, at the same time to the library. It doesn't seem to be the -- this is not the right process. I mean it goes to the review committee, there are reports written about that and if anything, at some point, the whole package with recommendations of the reviewers and so forth 10:39:00 10:39:02 10:39:06 10:39:09 10:39:14 10:39:18 10:39:20 10:39:29 10:39:31 10:39:33 10:39:35 10:39:40

would possibly make it then to the library as 10:39:43
a final result of a complete process. 10:39:46
Now, since this process was an ongoing 10:39:49
thing, prior to the review I would have certainly 10:39:52
not expected anybody to submit something to the 10:39:56
library. It may also be that the LHC Committee 10:39:58
at some point later, for instance at the 10:40:02
conclusion of the RD24 project, took the whole 10:40:05
package and submitted it to the library. I don't 10:40:09
know the exact process that happened here. 10:40:11

BY MR. BUROKER: 10:40:15

Q. Do you have any expertise or 10:40:15
knowledge about CERN library's procedures? 10:40:18

A. Not in depth. I'm using the 10:40:21
library of course, but we submit our documents to 10:40:23
our own libraries, but the procedures how 10:40:30
libraries work are relatively simple. 10:40:35

Q. Do you know whether the CERN 10:40:37
library, as part of its normal practice back in 10:40:38
1996, would receive copies of everything sent to 10:40:41
the HCCC (sic)? 10:40:44

MR. DAVIS: Objection; form. 10:40:48

BY MR. BUROKER: 10:40:50

Q. Excuse me to the LHCC. I used the 10:40:50
wrong acronym. 10:40:53

MR. DAVIS: Objection; form. 10:40:55

THE WITNESS: I would doubt that since you said "everything". 10:41:00 10:41:01

BY MR. BUROKER: 10:41:02

Q. Do you know whether, as part of the normal procedures, the LHCC would provide copies of status reports to the library? 10:41:02 10:41:05 10:41:10

A. I'm not aware that all my status reports -- and I wrote a lot of them -- for my own projects I had later for the LHC project were all submitted to the library, I'm not aware of that. Now, I haven't though done an in-depth search, but I would find it highly unusual and inappropriate in particular since I wasn't asked. 10:41:21 10:41:23 10:41:25 10:41:31 10:41:33 10:41:37 10:41:42

Q. Is there a physical library still at CERN? 10:41:44 10:41:49

A. Oh yes. 10:41:50

Q. And so you visited the library during the '96 to '98 timeframe? 10:41:50 10:41:53

A. Yeah, from time to time, it's pretty big. 10:41:57 10:41:58

Q. And at that time was there also a network-based access to the library's database, so that if somebody were looking to see what was available and you were in California, for 10:41:59 10:42:04 10:42:08 10:42:10

example, could you link in to find out what was 10:42:12
there? 10:42:15
A. I never did that from California, 10:42:16
certainly not when at CERN. I went there. 10:42:18
Whether they had an electronic index already at 10:42:22
that time I'm not sure, I don't remember. I 10:42:25
still remember they have even these huge rows, 10:42:28
where you have all these little library cards, 10:42:33
with the index and so forth as it used to be. 10:42:38
Q. Did you attempt to contact anyone 10:42:45
with a CERN library connection with trying to 10:42:48
determine whether or not this Bogaerts reference 10:42:51
was -- 10:42:57
A. I did not. 10:42:57
Q. -- publicly available? 10:42:58
Have you submitted documents to the CERN 10:43:00
library in the past? 10:43:04
A. Directly, no. And this is highly 10:43:08
unusual, wouldn't do that. The way it works is 10:43:11
the CERN library is -- a library usually doesn't 10:43:19
accept ordinary work in progress or status report 10:43:25
material. The library usually wants finalized 10:43:29
documents: a thesis, an approved paper. There is 10:43:33
this area of grey literature, which is what we 10:43:39
call preprints, almost the proof paper, so papers 10:43:41

submitted for acceptance. CERN has a rather complex way of accepting publications so, unlike in other areas where we have this rule of freedom to publish anything you want, at CERN you can't do that. If I wish to write a paper in the context of a CERN experiment it has to be submitted first to the committee inside CERN, the committee will review that, we're talking something like ten people typically on such a committee. The paper is being iterated many, many times, it can take half a year, sometimes a year before it's approved. Once it's approved it's submitted for publication with a CERN approval, and once the paper is accepted for publication then by the book or magazine, whoever publishes, Phys Ref Letters and so forth, then it would make its way into the library and that, again, only under certain conditions because there are publishing agencies which forbid that and then you find in the library only a reference saying if you want a copy of that document you have to either go to the publishing house. In case of Phys Ref Letters CERN of course has bought a license to that magazine. 10:43:44 10:43:49 10:43:54 10:43:59 10:44:03 10:44:05 10:44:07 10:44:09 10:44:11 10:44:13 10:44:19 10:44:22 10:44:24 10:44:29 10:44:33 10:44:39 10:44:44 10:44:46 10:44:49 10:44:52 10:44:55 10:44:57 10:45:02 10:45:09

Q. Wait, are you saying "list of 10:45:10

letters"? What are you saying? 10:45:11
A. Physical Review Letters. 10:45:14
Q. Okay, I apologize. She's not 10:45:15
getting it and we want a clear record. 10:45:17
A. That's fine, Phys Ref Letters is 10:45:20
the short form. I apologize for that. They are 10:45:25
always cited as that and this is -- 10:45:28
Q. Phys Ref, okay, I got you. 10:45:28
A. Yeah. Because they have very high 10:45:29
impact points, and this is, in physics, very 10:45:32
important to have a publication in Phys Ref. 10:45:34
But, for example, if you publish it in certain 10:45:38
magazines, they do not allow you to use it 10:45:43
anywhere else, you also have to buy then the 10:45:47
magazine and that means for this particular 10:45:50
magazine there is no electronic version, you have 10:45:52
to go to the CERN library and pull the physical 10:45:55
paper out of the shelf to be able to read it and 10:45:58
make copies and so forth. 10:46:03
There is a long and ongoing debate, not 10:46:04
settled, about all of this, because it turns out 10:46:07
that the electronic version of a paper often is 10:46:13
more expensive than just buying the paper version 10:46:16
of a magazine, but the paper version is highly 10:46:18
inconvenient because, you know, it takes a lot of 10:46:22

time before you have it and so forth. But the fact is, if all these conditions are met, a paper approved for publication is out there, it is real and the paper is part of the stuff the library buys anyway. I mean Phys Ref Letters costs something like 30 or 40,000 a year if I remember correctly, really expensive. Then you can have it in the library. It's not yet on the internet; only if CERN also acquired an internet license for that magazine and it is also available. 10:46:24 10:46:29 10:46:32 10:46:36 10:46:41 10:46:45 10:46:47 10:46:49 10:46:54 10:46:58

So, you see, this is absolutely a non-trivial thing and libraries have to be really, really careful. Imagine even just one version of a copyrighted paper ends up on the internet without approval, you immediately have all the litigation for damages and so forth. 10:47:00 10:47:03 10:47:06 10:47:09 10:47:13 10:47:15

Q. So I think that the question was whether you had ever submitted the document to CERN for publication and the answer was no, right? 10:47:20 10:47:23 10:47:26 10:47:30

A. I would submit it to the committee, the committee would publish it and then, as part of the automatic process, it would eventually end up in the library. So, strictly spoken, directly? No. Indirectly according to 10:47:30 10:47:31 10:47:33 10:47:36 10:47:39

the procedure set forth? Yes. 10:47:42
Q. So some documents that you've 10:47:44
submitted to committee have been published or are 10:47:47
part of the publications of the CERN library but 10:47:53
through the committee process; is that right? 10:47:55
A. Yeah. 10:47:57
MR. DAVIS: Objection; form. 10:47:57
BY MR. BUROKER: 10:47:57
Q. And that's the same committee, the 10:48:00
LHCC Committee or is there a different Committee 10:48:02
you're referring to? 10:48:04
A. No, no, no totally different. The 10:48:04
LHCC Committee is only there to monitor the 10:48:06
process of development work for LHC-related 10:48:08
experiments or accelerator, okay? Now we have 10:48:13
LHC in operation since a couple of years and 10:48:23
experiments are taking data and analyzing data. 10:48:31
So, for instance, I'm a member of the ALICE 10:48:33
Collaboration. This is 1,100 scientists. So 10:48:36
a publication like this one, has a two- or 10:48:39
three-page front page stating all the times -- 10:48:43
right, 1,000 names is a lot of stuff -- with all 10:48:45
the affiliations, and inside ALICE we have 10:48:49
a Publication Committee which has at least five 10:48:56
or six subgroups focusing at different subfields 10:49:01

of the physics which ALICE does. And every 10:49:04
single paper goes through that process. There is 10:49:08
even a mitigation framework there. So, for 10:49:13
example, if the author doesn't agree with what 10:49:17
the committee wants changed, then it's escalated, 10:49:19
worst case, to the ALICE Management Board and 10:49:22
a decision is being made and so forth. But this 10:49:25
is now a scrutiny process which is inside ALICE. 10:49:28
On top of that it's really highly complicated. 10:49:33
If you have what is considered 10:49:38
a discovery-level publication, you found a new 10:49:42
particle, even then ALICE cannot publish it. 10:49:44
Then it goes to the CERN Director and the CERN 10:49:48
Director will put a hold on that paper until he's 10:49:52
convinced that (a) it is absolutely solid and 10:49:55
correct and (b) if there is the possibility of 10:50:00
a second CERN experiment measuring it he likes to 10:50:03
see them measuring it, too, to have a second 10:50:06
validation. You may remember the cold fusion 10:50:09
case which happened in Germany and somebody made 10:50:12
huge noise, big press media, about having found a 10:50:16
way to do fusion basically in the laboratory and 10:50:22
that was a hoax; big embarrassment for everybody. 10:50:26
So CERN has put a very, very high level of 10:50:30
scrutiny to avoid this from happening and yet you 10:50:35

may have noticed the big press campaign about 10:50:38
CERN having measured a particle traveling faster 10:50:40
than the speed of light, which was wrong and yet 10:50:42
it went out. So even there the scrutiny failed. 10:50:46

Q. So I'm going to ask you to listen 10:50:54
to my questions and answer those questions. I 10:50:55
know you like to go on and explain your answers, 10:50:58
and I mean your counsel can ask you follow-up 10:51:01
questions if he needs to. My question was: was 10:51:03
it a different committee? 10:51:07

A. Yes. 10:51:08

Q. Thank you. In the 1996 timeframe, 10:51:08
when the Exhibit 1011 was submitted, do you know 10:51:21
what the procedure was for LHCC to submit 10:51:27
a document to the library? If there is such 10:51:35
a procedure? 10:51:38

MR. DAVIS: Objection; form. 10:51:39

THE WITNESS: No explicit set of rules 10:51:45
comes to my mind, except that it's the same 10:51:49
standard procedure how libraries worked. No 10:51:53
particular rules I remember. 10:51:56

BY MR. BUROKER: 10:52:02

Q. Do you recall personally 10:52:02
submitting this report to anyone after it was 10:52:05
submitted to the LHCC? 10:52:11

A. No.

Q. Do you know whether Dr. Müller submitted this document to anyone other than the LHCC at that time in 1996?

A. No, and I was surprised because there were quite a few confidentiality agreements associated with this.

Q. Right. So you do give some testimony in your declaration about confidentiality.

Paragraph 170, for example, of the '814 declaration says that:

"... it is likely that the RD24 status report would NOT have been published on that date because it was subject to confidentiality agreements."

A. That's correct.

Q. You don't cite to what those confidentiality agreements are in this declaration, correct?

A. Yes, correct.

Q. And the document itself doesn't have any confidentiality labels that I've been able to find. Have you been able to find any?

A. I did not, no. Although I didn't

explicitly look for them but no. 10:53:31

Q. And you agree that, as of 2014 at 10:53:58
least, or 2015, this document is now publicly 10:54:04
accessible, correct? 10:54:09

MR. DAVIS: Objection; form. 10:54:12

THE WITNESS: The big question is now 10:54:16
what do you mean with "this document"? If you 10:54:18
mean the version with the CERN library stamp as 10:54:20
it was then, yes, one can find it now through the 10:54:24
internet on the CERN library pages. I Googled 10:54:35
for it and I did find it, yes. 10:54:40

BY MR. BUROKER: 10:54:43

Q. Okay. And you don't have any 10:54:43
information about when between 1996 and 2014 this 10:54:44
did become publicly available, correct? 10:54:54

A. Correct, I cannot tell you the 10:54:56
date. 10:54:57

Q. And Dr. Müller couldn't tell you 10:54:59
the date, correct? 10:55:02

A. No. Yeah, correct. Yes, I should 10:55:03
say something here. You've just asked a negative 10:55:07
question, right? "Could not". 10:55:12

Q. Yeah, and if you want to -- 10:55:14

A. No, no, to make it clear, I tried 10:55:16
to be very correct here and there is a little but 10:55:19

nasty pitfall; the correct answer to a negative question in the U.S. is "no". The affirmative answer to a negative question is "no" -- is "yes", sorry, in Germany it is "no". 10:55:23 10:55:28 10:55:31 10:55:35

Q. Okay, let me ask it again. 10:55:37

Did Dr. Müller know when this document became publicly available? 10:55:39 10:55:45

A. He could not tell, arguing, "This is almost 20 years ago, how would I know? This is more than 20 years ago when I wrote this, how would I know?" 10:55:46 10:55:49 10:55:53 10:55:56

Q. There's some discussion in the declaration about -- I guess it starts on paragraph 174 -- about the internet linking of this report, or a copy of this report. So I want to ask you some questions about that. 10:56:14 10:56:15 10:56:18 10:56:25 10:56:32

You say in your declaration at paragraph 176 that you believe: 10:56:35 10:56:38

"... that the RD24 status report was ... 10:56:42 10:56:42

-- which is the Bogaerts reference, and let me find the right language: 10:56:46 10:56:50

"... inadvertently linked to a public web page on Mr. Müller's private web server and was later removed." 10:56:52 10:56:55 10:56:58

Do you see that at the end of 176? 10:56:59

A. Yes. 10:57:05

Q. Did you discuss this piece of information with Mr. Müller? 10:57:14 10:57:16

A. No. 10:57:17

Q. You didn't ask him? 10:57:18

A. I did not. I didn't see any point because -- no, I didn't ask, no. 10:57:19 10:57:22

Q. What is the basis for your statement that you believe it was "inadvertently linked"? 10:57:27 10:57:29 10:57:33

A. The machine sunshine is one of the machines that Hans Müller used at that time. Although it's long ago I still remember that because it was these nice shiny flat boxes and quite expensive, I wanted one, too, but at first I didn't have one, so these are the things you remember. And since it's the machine built by Sun MicroSystems he called them sunshine and the other one was called sunrise, being the machines of the RD24 project basically his personal machines he used to work with. 10:57:37 10:57:44 10:57:50 10:57:52 10:57:57 10:57:59 10:58:01 10:58:06 10:58:09 10:58:13 10:58:17

And you see that the URL specified here has this ":8080" after it. This is the URL or HTTP syntax which specifies the port number. The 10:58:18 10:58:30 10:58:38

port number is a number used in the internet to identify a particular sub-functionality of a computer. The official port number for internet web access -- the World Wide Web -- is port 80. Most of the computers at the time came already with a private web server built in, used for all sorts of maintenance functionality and so forth. And usually if you just wanted to set up something for your own contacts and work you might use a different port number and Hans Müller invented 8080. Obviously it is clear where it comes from. This number has to be between one and 65,535, so you have roughly 65,000 options. However, the internet search engines usually use the internet addresses, so port 80, right? So if you typed www.ibm.com, you'd definitely end up at a port of 80. So, from that point of view an ordinary search engine -- and one should know at that time there were not that many search engines, I'm not sure Google already existed at all -- that would look for any other port. And it would not be successful if you were to try to just screen whether or not a computer is using another port because that would be detected by the computer security infrastructure and you

would be considered a hacker and you would be blocked completely. CERN does that completely automatically. 11:00:23 11:00:27 11:00:29

So for this document to be found there must have been -- by any web crawler, as these machines are being called, you know, which go on websites, try to read everything, store it somewhere and then follow links, the only reasonable way for this to be done, would be that some link somewhere would have redirected to this point. This is the rationale behind that statement. 11:00:32 11:00:34 11:00:40 11:00:43 11:00:47 11:00:49 11:00:53 11:00:58 11:01:00

Q. Okay, but the fact of the matter is it was linked and captured by the internet archive in 1996, right? 11:01:00 11:01:02 11:01:07

A. That document was submitted, yes, although this is, if I remember correctly, only part of it some different pages, but they have certain fraction of it, yes. 11:01:10 11:01:13 11:01:16 11:01:19

Q. Well, they have a postscript file that if you click on it you get the entire document, correct? Did you try it? 11:01:24 11:01:26 11:01:29

MR. DAVIS: Objection; form. 11:01:30

BY MR. BUROKER: 11:01:32

Q. Did you personally visit this U -- 11:01:32

looking in paragraph 174, there's a URL, there's two URLs. The top one -- excuse me, the second one is a postscript file, correct? 11:01:37 11:01:47 11:01:52

A. The second? 11:01:55

MR. DAVIS: Objection; form. 11:01:56

BY MR. BUROKER: 11:01:59

Q. The second link? 11:01:59

A. So the second link and you're referring to the HTTP "web.archive.../web" and then all sorts of long numbers, "sunshine.cern.ch:8080...RD2496_1.ps". Yeah, the extension ".ps" indicates it's be to a postscript file. 11:02:00 11:02:03 11:02:07 11:02:10 11:02:17 11:02:20

Q. Right. And did you visit that URL? 11:02:20 11:02:23

A. I'm not sure. 11:02:24

Q. And did you visit that URL and click on that link and see what response you got back? 11:02:27 11:02:32 11:02:34

A. I can't tell you. I did click on a few of those references but for this particular one I can't tell you. 11:02:38 11:02:42 11:02:48

Q. And a postscript file is an Adobe file format that builds a PDF, correct? 11:02:49 11:02:54

A. No. 11:02:58

Q. What is a postscript file? 11:02:58

A. At the time we're discussing here, 11:03:07
1996, PDF did not exist. Postscript is a page 11:03:09
description language, which was invented by Adobe 11:03:13
also, which basically has all elements to 11:03:16
basically print any kind of document, any form, 11:03:22
any kind of graphics, whatsoever. It's a page 11:03:26
description language in the strictest sense, it 11:03:33
has commands in there, certain rules. So, for 11:03:36
example, if you have a text and it has to be 11:03:41
modified then there are commands saying make this 11:03:42
boldface and underscored and what-not. So the 11:03:45
text of the document is basically encapsulated 11:03:47
inside the whole postscript context. There is 11:03:49
a lot of declaration stuff at the beginning, if 11:03:55
you look through it. And, in particular, if you 11:03:57
look at the text version of this document you 11:03:59
will find that you will not be able to read this, 11:04:02
right? Because the text basically disappears in 11:04:04
all the commands. 11:04:09

PDF -- the portable data format -- is 11:04:10
something which was introduced by Adobe later for 11:04:13
many reasons. One reason was that postscript 11:04:18
turned out not being as portable and as easily 11:04:23
reproducible as people like them to -- I still 11:04:27

remember infinite sessions where we spent hours 11:04:31
because the printer just wouldn't print that 11:04:35
file. It looked fine on screen, you saw 11:04:37
everything, it was perfect, but the printer 11:04:41
wouldn't print it, or what came out was complete 11:04:42
nonsense. Even when I went back to Heidelberg, I 11:04:45
still remember a lot of effort we had to put in 11:04:52
because, for example, it would happen that 11:04:56
a printer disregarded the first command saying, 11:04:58
"This is postscript", and then you would end up 11:05:01
having 500 pages of postscript commands for 11:05:04
a single-page document because sometimes it would 11:05:07
even, you know, one-command-per-line kind of 11:05:10
nonsense. All of this was a problem because the 11:05:12
document which can't reliably print and 11:05:16
reproducibly print in every country, big issues 11:05:18
between U.S. letter format and European A4, that 11:05:21
was solved by introducing PDF, the really 11:05:25
portable data format. And postscript is 11:05:28
basically not being used anymore. There are 11:05:31
converters which are automatically evoked if you 11:05:34
open a postscript file and this was why people 11:05:37
tend to believe that postscript is basically part 11:05:41
of PDF but it's not. 11:05:44

Q. Okay, but in '96, if you had 11:05:46

a postscript file in the relevant linked 11:05:48
references, you could generate something to be 11:05:53
printed? Is that what the purpose of postscript 11:05:56
files was? 11:05:59

MR. DAVIS: Objection; form. 11:06:00

THE WITNESS: You would have to 11:06:01
download it and then depending on what kind of 11:06:06
web browser you had, usually not automatically at 11:06:09
this time if I remember correctly, you would have 11:06:12
to have a postscript viewer to view this 11:06:14
postscript file to have it on screen, and you 11:06:17
would have to have a postscript-enabled printer 11:06:19
which would understand postscript and those 11:06:22
printers were more expensive because they needed 11:06:24
a postscript interpreter which is a rather 11:06:26
complex piece of software and lots of memory for 11:06:30
it to be able then turn this into something on 11:06:32
paper. 11:06:35

BY MR. BUROKER: 11:06:46

Q. Let me show you what's been 11:06:46
previously marked as Exhibit 2026 in the '1469 11:06:48
IPR proceeding. This is an affidavit of 11:06:59
Christopher Butler from the Internet Archive. 11:07:02
Have you ever viewed this document as one of the 11:07:05
things you considered? 11:07:08

A. I have looked at it, yes. 11:07:09
Q. Okay, and he attaches materials 11:07:11
that were from the Internet Archive from October 11:07:14
-- strike that -- from January 26th, 1997; is 11:07:26
that correct? 11:07:32
MR. DAVIS: Objection; form. 11:07:35
THE WITNESS: Which particular page are 11:07:38
you now referring to? 11:07:40
BY MR. BUROKER: 11:07:42
Q. I strike that. I'm more 11:07:42
interested in the documents that were 11:07:43
from October 29, 1996. So it's the one that 11:07:48
starts on page 11 of this document. 11:07:53
MR. DAVIS: Objection; form. 11:07:59
BY MR. BUROKER: 11:08:01
Q. 011. So, the question is: in 11:08:03
paragraph 6 of his affidavit, he says: 11:08:23
"Attached ... as Exhibit A are true and 11:08:26
accurate copies of printouts of the Internet 11:08:28
Archive's records of the HTML and PDF files for 11:08:32
the URLs and the dates specified in the footer of 11:08:36
the printout (for HTML) or on the attached 11:08:40
coversheet (for PDF)." 11:08:42
MR. DAVIS: Objection; form. 11:08:44
/// 11:08:46

BY MR. BUROKER: 11:08:46
Q. Is that what it says? 11:08:46
A. This is what is written here, yes. 11:08:49
Q. Okay. So on page 11 there's a URL and that's the URL that we were just talking about from your declaration; is that right? 11:08:53 11:09:01 11:09:03
MR. DAVIS: Objection; form. 11:09:07
THE WITNESS: I would have to compare. If you say so. 11:09:09 11:09:12
BY MR. BUROKER: 11:09:15
Q. It was paragraph 174. 11:09:15
A. Yes. 11:09:17
Q. Okay. And then what is attached next, on pages 12 through 49, appears to be the RD24 status report that is the same as the EMC Exhibit 1011 without the library stamp. Do you agree? 11:09:33 11:09:36 11:09:46 11:09:55 11:09:58
MR. DAVIS: Objection; form. 11:09:59
THE WITNESS: By looking at it I would say so, yes. However, I have not done a direct one-to-one comparison. There may be an earlier version, but since it's dated October 2nd, I would assume so. But please note this is not the entire document, the document was broken up into several pieces, so there is an RD2496_1, _2, 11:10:03 11:10:06 11:10:10 11:10:12 11:10:16 11:10:18 11:10:20

_3.

BY MR. BUROKER:

Q. Right.

A. And although I don't know the reason -- _4 even. Let me see, is there another one? I don't remember the reason for doing this. The most likely cause would be this document is filled with pictures and pictures were real full having postscript files to print, or printers to choke when the whole postscript file was submitted, so postscript files then were chopped up into smaller pieces, let alone to be able to print the stuff which would print and isolate the potential error. So this is basically fragments of the whole document.

Q. Right.

A. But they are all there.

Q. Right. In fact there are eight. Page 46 of this has the file header for RD2496_8.ps, correct?

A. Eight, yeah, you're right.

Q. So if you took the pieces of the document from each of the different RD2496 postscript files and put them together, did you do a comparison as to whether that compilation is

the same as Exhibit 1011 minus the CERN library stamp? 11:11:45 11:11:50

MR. DAVIS: Objection to form. 11:11:51

THE WITNESS: I did not do an in-depth comparison whether or not they are word by word the same, but I did check that overall they looked to be the same, same page numbers. Nothing obvious came to mind and I would not see any reason why this would be a different version. 11:11:53 11:11:57 11:12:00 11:12:05 11:12:08 11:12:12

BY MR. BUROKER: 11:12:15

Q. Right. And so for them to have been -- for these postscript files to have been gathered by the Internet Archive on October 29th, 1996, by that time somebody would have had to place those postscript files on the sunshine.cern.ch:8080 server, correct? 11:12:15 11:12:18 11:12:24 11:12:27 11:12:34 11:12:37

MR. DAVIS: Objection; form. 11:12:48

THE WITNESS: This archive claims that these documents were downloaded from sunshine.cern.ch:8080. This is what I understand. 11:12:50 11:12:54 11:13:00 11:13:05

BY MR. BUROKER: 11:13:06

Q. And you have no reason to doubt the Christopher Butler affidavit, do you? 11:13:06 11:13:07

A. No, I mean I believe he signed 11:13:10

that under oath, right? 11:13:12

Q. So do you know who put those postscript files on that sunshine.cern.ch:8080 server? 11:13:14 11:13:19 11:13:25

A. I don't know but it would be relatively likely that this was Hans Müller, and it was also very possible that -- because these documents have a certain size particular to postscript -- that this was the place where everybody was referring to to look at the final document and to say it's all right as part of the work in progress. But remember this is the private web page of the RD24 and not an official generic searchable web page. 11:13:28 11:13:31 11:13:40 11:13:43 11:13:45 11:13:49 11:13:52 11:13:56 11:13:58 11:14:03

Q. Well you say it's private but it's on the CERN server, right? 11:14:06 11:14:08

A. CERN has about 10,000 computers. So it's one particular computer of one person working at CERN -- there are 3,000 employees -- who is using this on a sub-web page which is not part of the official port 80 web pages. So if you would go to www.cern.ch you would not find this, right? This is something else. 11:14:11 11:14:14 11:14:19 11:14:24 11:14:31 11:14:35 11:14:38

Q. Well, but CERN owned the computer, right? 11:14:42 11:14:44

MR. DAVIS: Objection; form. 11:14:44

BY MR. BUROKER: 11:14:44

Q. You're trying to draw some distinction and say it's private, but this is a cern.ch address. 11:14:49 11:14:50 11:14:55

A. Yeah, but the conclusion you're trying to draw is really wrong. I have computers at CERN worth millions of euros which are owned by the government in Germany because they're paid for by the German Research Council BMBF, but they are at CERN. And since they are for a CERN experiment they are, of course, operating in the CERN computer contacts and if you want to get them they have a CERN network address. 11:15:00 11:15:02 11:15:07 11:15:10 11:15:12 11:15:16 11:15:19 11:15:23 11:15:25

Q. But Müller chose to put these on an address that was a cern.ch address and not, you know, drmüller.com or some other URL he could have used, right? 11:15:29 11:15:35 11:15:38 11:15:44

MR. DAVIS: Objection; form. 11:15:45

THE WITNESS: Every computer at CERN -- I mean maybe we should enter briefly into a discussion how networks work because I believe there is a misunderstanding here. 11:15:51 11:15:54 11:15:56 11:16:01

If I would bring my laptop -- 11:16:05

BY MR. BUROKER: 11:16:07

Q. Well that's not an answer to my question, sir. I asked you a question about whether Mr. Müller or Dr. Müller choose to put these on a cern.ch addressed server. 11:16:07 11:16:09 11:16:11 11:16:14

MR. DAVIS: Objection; form. 11:16:19

THE WITNESS: He put it on a computer which belonged to the RD24 project which was located at CERN and thereby had a CERN network address, like every guest or every person visiting CERN having a CERN network address. Like every person in this room going on to the network, getting a network address in the domain of your law firm. 11:16:21 11:16:23 11:16:30 11:16:33 11:16:37 11:16:42 11:16:44 11:16:48

BY MR. BUROKER: 11:16:52

Q. Right. And so if I posted something on my firm's network, it wouldn't be my private server, just as this was not really his private server. It's a piece of equipment owned by his employer and on his employer's URL, correct? 11:16:52 11:16:55 11:16:57 11:17:00 11:17:03 11:17:08

MR. DAVIS: Objection; form. 11:17:09

THE WITNESS: This is what I tried to outline. CERN is not just an employer which owns everything which is part of CERN. CERN is an international organization with lots of highly 11:17:11 11:17:12 11:17:17 11:17:20

complicated contracts with lots of entirely autonomously operating organizations. So, for example, the ALICE experiment has nothing to do with CERN although it is located at CERN. We have our own rules, we even have our own bank accounts at CERN, although they are under diplomatic immunity. Nobody can get to these accounts unless the account owner, in one case myself, approves that. Same for the computers. If there is a particular project it has its own set of contacts and ownerships and the fact that the computer are located at CERN only means that they get a CERN address but that doesn't mean that the contents in these computers are owned by CERN or necessarily the computer is owned by CERN. The ownership of sunshine I don't know. RD24 had different funding sources and how the money came together to, for instance, buy those machines, I can't tell at this point, but you cannot automatically draw the conclusion that this is an employee-employee relationship and everything that is under the CERN, inside the CERN domain is owned by CERN.

BY MR. BUROKER:

Q. But you've drawn a conclusion and

given an opinion under oath that it was his private server; is that correct? 11:18:41 11:18:43

A. Private server in the sense of the RD24 project, yes. Not private server in the sense he owned it personally privately. This is the RD24 project and in this context his private server, yeah. 11:18:45 11:18:47 11:18:50 11:18:52 11:18:55

Q. Often private is used to distinguish between public; was that the distinction you were trying to draw? Or what was the reason why you said it was a private server? 11:19:00 11:19:03 11:19:05 11:19:08

MR. DAVIS: Objection to form. 11:19:12

THE WITNESS: Both. This is a machine belonging to the RD24 project and the information on there was for the RD24 project, inside the RD24 project, and not for the public and consequently, therefore, I used the word "private". 11:19:18 11:19:21 11:19:26 11:19:31 11:19:36 11:19:39

BY MR. BUROKER: 11:19:39

Q. Was he an employee of CERN? 11:19:40

A. Hans Müller was an employee of CERN, correct. 11:19:43 11:19:45

Q. Is he still an employee of CERN? To your knowledge obviously? 11:19:46 11:19:48

A. He has reached the age of 11:19:50

retirement. He may still be or already have retired but he is still working at CERN, which is rather common. People do research because they like to do that and they keep doing this after their retirement. So he may or may not be at this point. 11:19:52 11:19:57 11:20:01 11:20:07 11:20:09 11:20:12

Q. Just to be clear, so we know what the facts are. So what's your understanding as to who owns the cern.ch domain? 11:20:13 11:20:16 11:20:19

MR. DAVIS: Objection to form. 11:20:23

THE WITNESS: The cern.ch domain is registered by the organization CERN. So from that point of view you can argue that CERN owns it. 11:20:28 11:20:33 11:20:35 11:20:37

BY MR. BUROKER: 11:20:50

Q. And if I visit a www.cern.ch URL, is that going to be a CERN website? 11:20:50 11:20:59

A. That would be the CERN official website, organized by the CERN public relations department, run by the CERN IT department. 11:21:03 11:21:05 11:21:09

Q. And the contents of that website would be served off of a CERN server; is that correct? 11:21:12 11:21:13 11:21:13

A. That I would assume so to be correct. 11:21:19 11:21:21

Q. Are you familiar with the URL cds.cern.ch? 11:21:23 11:21:25
A. Where is that? 11:21:32
Q. I don't know if it's in your declaration or not. 11:21:35 11:21:37
A. Outside the context I may or may not know, I would need to look at it to be sure. 11:21:39 11:21:41
Q. It doesn't immediately come to mind as being the CERN Document Server that's associated with the CERN library; is that correct? 11:21:47 11:21:49 11:21:54 11:21:57
A. Well, the CERN Document Server I am of course aware, yeah, sure. 11:21:58 11:22:00
Q. Okay, so cds.cern.ch is affiliated with the CERN library; is that correct? 11:22:02 11:22:07
MR. DAVIS: Objection; form. 11:22:11
THE WITNESS: I would assume so. I mean the CERN Document Server means something to me. The short form, how they code that as a URL, I do not know. CERN has a rather complicated document management system which we use. Many, many complex links between different pages which are all residing inside this framework. 11:22:12 11:22:14 11:22:16 11:22:21 11:22:24 11:22:30 11:22:33
BY MR. BUROKER: 11:22:40
Q. And I think you said before, but 11:22:40

let me just clarify it, who owns the computer server that provided the content in the '96 timeframe related to the sunshine.cern.ch URL? 11:22:42 11:22:45 11:22:51

MR. DAVIS: Objection; form. 11:22:58

THE WITNESS: To be correct, I cannot tell. It would be the RD24 project which is a part of CERN but had its own budget, and how the exact financial contributions came about I'm quite sure Dolphin invested something and other companies did, which is very standard at that stage in time, even today; CERN has an entire working group doing this kind stuff. And then Hans Müller may have decided one or the other way how funds are being put together in order to pay this. So that I can't tell after 20 years. 11:23:02 11:23:03 11:23:07 11:23:11 11:23:14 11:23:17 11:23:20 11:23:24 11:23:27 11:23:29 11:23:32

BY MR. BUROKER: 11:23:37

Q. Do you know who had access in 1996 to the sunshine.cern.ch server? 11:23:37 11:23:40

MR. DAVIS: Objection; form. 11:23:43

THE WITNESS: Hans Müller certainly. I would assume also Hans Bogaerts -- sorry Andreas Bogaerts -- B-o-g-a-e-r-t-s -- who is also an author here. These were two jointly leading the RD24 project. Probably some of the people who worked at CERN with Hans Müller. I 11:23:48 11:23:49 11:23:59 11:23:59 11:24:07 11:24:10

don't remember having access except for these private web pages, but I can't really give a complete list. 11:24:12 11:24:16 11:24:20

BY MR. BUROKER: 11:24:20

Q. Okay. So I just want to clarify that. You do recall visiting the sunshine.cern.ch:8080 pages? 11:24:22 11:24:24 11:24:27

A. I probably did. 11:24:32

Q. Is it typical in referee publications to cite to something that's confidential in your experience? 11:24:41 11:24:49 11:24:50

MR. DAVIS: Objection; form. 11:24:52

THE WITNESS: Not really, because a citation is there to give a second reference to back up an argument and if it's confidential and you cannot use this it would be difficult. 11:24:58 11:25:01 11:25:04 11:25:07

But it can happen that such citations are being made and certain particular access is given. So, for example, we have these cases happening from time to time if there is a PhD thesis written as a joint project with industry, and the thesis contains material which is, for example, subject to a patent just being in the process of being filed and the thesis is declared confidential, although a thesis has to be 11:25:16 11:25:20 11:25:24 11:25:27 11:25:30 11:25:35 11:25:38 11:25:42 11:25:45

published one can put a certain timeframe on it 11:25:47
saying it will remain unpublished for a certain 11:25:50
time until, for example, all the IP has been 11:25:53
filed and the submission of the thesis is not 11:25:56
damaging any more to the IP. So this "no" has to 11:25:58
be taken with a grain of salt. 11:26:07

(Exhibit No. EMC 1027 was marked for 11:26:07
identification.) 11:26:20

BY MR. BUROKER: 11:26:20

Q. And I believe we're on the same 11:26:20
numbering scheme for both IPRs on the 1000 11:26:21
series, so this is 1027 in both proceedings. 11:26:25
Actually, yeah, we'll just make it 1027 in both 11:26:31
proceedings just to make it easier. 11:26:38

MR. DAVIS: Okay. I'm going to make 11:26:39
some evidentiary objections. It's outside the 11:26:40
scope of direct of institution. I can't tell if 11:26:43
it's incomplete or not. I think it's irrelevant, 11:26:48
may be prejudicial, likely hearsay, lacks 11:26:54
authentication and may contain improper opinion 11:26:58
evidence. 11:27:03

BY MR. BUROKER: 11:27:07

Q. Okay, Dr. Lindenstruth, have you 11:27:07
ever seen this before? 11:27:11

A. I do not remember. 11:27:13

Q. Is the Hans Müller the same Hans Müller we've been talking about? Was he affiliated with the CERN EP Electronic Design Group?

A. Well I mean it states so on this document so I have no reason to doubt that, although CERN is constantly restructuring. The EP Group was or is a really large group. It is well possible that he was a member of that group at that time.

Q. Do you know what an LHC-B note is?

A. You're referring to the header of the document LHC-B?

Q. Yes, the header says:

"LHC-B Note 98-030."

So I was asking if you knew what an LHC-B note is.

A. CERN has four major experiments for its LHC accelerator, right? One has to disentangle the accelerator, we call that the machine, and then the experiments. The physics is done at the experiments. There are four experiments: ALICE; ATLAS; CMS; and LHC-B. LHC-B, an obviously very creative name, was chosen because LHC studies the weak interaction,

which is very important for understanding some of 11:28:59
the fundamental principles of our being here. 11:29:03
The B meson -- m-e-s-o-n -- is a particle which 11:29:09
decays weakly interacting and is extremely rare 11:29:18
and one needs these extremely powerful 11:29:24
accelerators to create them and then LHC-B was 11:29:27
built to basically study the decay of this B 11:29:31
meson. So since it's the LHC-B experiment, then 11:29:35
you see there are variants of noting, the title 11:29:39
says "LHCb" without dash, the note says "LHC-B" 11:29:44
with a dash. I assume this is a note of the 11:29:47
LHC-B experiment with a reference number. If it 11:29:51
was a document for the ALICE experiment, it would 11:29:58
be "ALICE Note" with such a number and so forth. 11:30:00

Q. Well who are these notes -- what 11:30:03
are these notes created for? 11:30:05

MR. DAVIS: Objection; form, outside 11:30:08
the scope. 11:30:11

THE WITNESS: Now, yeah, I'm not 11:30:13
a member of the LHC-B collaboration and I'm 11:30:15
seeing this for the first time. I can only draw 11:30:18
a conclusion from my experience how it works in 11:30:22
ALICE experiment, which is not uncommon. 11:30:25
Standard procedure is if you wish to make 11:30:30
a statement to the collaboration -- we're 11:30:33

talking, again, this group preparing the experiment -- saying, "This is the particular way something could work, this is a suggestion to solve a particular problem", then normally one writes up a note, which is basically an internal paper, which is submitted to that particular collaboration for review. 11:30:36 11:30:40 11:30:44 11:30:51 11:30:54 11:30:59 11:31:05

Notes are, as far as I know, never publications, they are used for internal -- they are made for internal use as a reference to discuss something particular. 11:31:11 11:31:14 11:31:15 11:31:18

BY MR. BUROKER: 11:31:27

Q. So, if you look at the references in this document. Reference 6 cites to the RD24 status report 1996, LHCC 96-33 October 1996, and then it's got the URL http://sunshine.cern.ch: 8080/RD24/rd24.html. Do you see that? 11:31:28 11:31:29 11:31:40 11:31:48 11:31:59

A. Yeah. 11:32:07

Q. So in 1998, in a note to the LHC-B, Hans Müller is citing to that sunshine.cern.ch:8080 server reference which appears to have the RD24 status report from 1996, correct? 11:32:08 11:32:14 11:32:17 11:32:23 11:32:27

MR. DAVIS: Objection; form. 11:32:28

THE WITNESS: Well it is printed here. 11:32:31

More I cannot say about that. 11:32:33

BY MR. BUROKER: 11:32:37

Q. That doesn't suggest to you -- well, first of all, you have never this document before? 11:32:37 11:32:38 11:32:41

A. No, I don't think so. 11:32:42

Q. Okay. So you didn't consider this in your declaration when you gave the opinion you thought that the RD24 document was kept confidential, correct? 11:32:44 11:32:46 11:32:50 11:32:53

In other words, you didn't have this when you made that determination? 11:32:56 11:32:57

A. Your second statement is correct, yes, I didn't have this when I made my declaration. 11:33:00 11:33:01 11:33:05

Q. Okay. And reference number 18 in this list of references also says: 11:33:05 11:33:09

"Applications of SCI to Data Acquisition at LHC ..." 11:33:12 11:33:21

-- which is the same title as Exhibit 1011, the RD24 status report, right? 11:33:22 11:33:25

MR. DAVIS: Objection to form. 11:33:28

THE WITNESS: Yeah, but I mean this is only referencing the RD24 home page, which is still using this private port number on the 11:33:36 11:33:37 11:33:41

website of Hans Müller, yeah. On this sunshine machine, yeah. 11:33:47 11:33:51

BY MR. BUROKER: 11:33:53

Q. All right, but he's citing to this port on this URL to a working group that's not the RD24 working group, he's citing it to the LHC-B group, correct? 11:33:53 11:33:56 11:34:02 11:34:05

A. Yet another CERN internal working group, yeah. 11:34:10 11:34:12

Q. So at a minimum he doesn't think that the document is confidential only to the RD24 working group? 11:34:13 11:34:14 11:34:17

MR. DAVIS: Objection to form. 11:34:19

BY MR. BUROKER: 11:34:21

Q. Correct? 11:34:21

MR. DAVIS: Calls for improper opinion evidence. 11:34:22 11:34:24

THE WITNESS: I mean, since you're referring several times to confidentiality, I should probably outline why I said that this is subject to confidentiality. 11:34:32 11:34:34 11:34:36 11:34:41

BY MR. BUROKER: 11:34:43

Q. Your counsel can ask you that question, I want an answer to my question which is that this document suggests that at least 11:34:43 11:34:44 11:34:46

Mr. Müller didn't believe that the RD24 status report had to be kept confidential within the RD24 working group because he cited it to an outside CERN group. 11:34:55 11:34:59 11:35:00 11:35:04

A. This is a CERN group. 11:35:08

Q. To another CERN group? 11:35:09

MR. DAVIS: Objection; form. And I maintain my evidentiary objection. 11:35:09 11:35:11

THE WITNESS: Again, it all depends on the particular confidentiality agreement which was signed. 11:35:18 11:35:20 11:35:21

BY MR. BUROKER: 11:35:23

Q. I'm just talking about, doesn't this suggest that at least Dr. Müller -- I said Mr. Müller it's Dr. Müller -- he has cited the RD24 status report to a different working group within CERN, correct? 11:35:23 11:35:25 11:35:29 11:35:32 11:35:36

MR. DAVIS: Objection; form. 11:35:41

THE WITNESS: That document was given to apparently somebody else, a different group inside CERN working under possibly the same confidentiality requirements. 11:35:44 11:35:49 11:35:52 11:35:58

BY MR. BUROKER: 11:36:03

Q. Do you know how many people were involved in the LHC-B working group in 1996 to 11:36:03 11:36:04

1998?

A. I do not. I see this document for the first time, I can't tell you.

Q. But this is a different question. Do you know, based on your work at CERN, do you know how many people were involved in the LHC-B working group in the '96 to '98 timeframe?

A. I mean it would have to be the group focusing at data acquisition and online data selection. I don't know the size of that group. From my experience it would be a rather small group, handful of people. But this is a guess and I don't wish to raise guesses here, so I can't give you a clear answer as how many people have been involved here, but we're not talking huge collaborations.

Q. Do you know if Dr. Müller was involved in both RD24 and the LHC-B working groups?

A. I mean, in general, these RD projects were not there to work for any particular experiment, they were there to solve generic problems for basically the entire LHC project. This is why they're called RD and not experiment A, B, C, D, right? And so it was well

within his obligations to, let's say, market the technology to possibly interested other groups helping them to solve their particular computing problems. So apparently he's trying to address an issue which is particular for the LHC-B experiment, showing a potential solution. But without referring to this document in depth -- and I would have to read it carefully, we're talking some 19 pages -- I can't tell more. 11:37:29 11:37:34 11:37:39 11:37:42 11:37:50 11:37:56 11:38:00 11:38:03 11:38:05

(Brief pause to re-establish realtime connections.) 11:39:39

BY MR. BUROKER: 11:39:39

Q. Dr. Lindenstruth, I want to turn you to page 8 and paragraph 20 of your '814 declaration. 11:39:40 11:39:40 11:39:45

So the first sentence says you understand that in Inter Partes Review, the claim terms are to be given their broadest reasonable interpretation in light of the specification, correct? 11:39:57 11:40:00 11:40:03 11:40:06 11:40:08

A. Yeah. 11:40:09

Q. And that's your understanding -- 11:40:09

A. Yeah. 11:40:12

Q. -- provided by counsel, correct? 11:40:12

A. (The witness nodded.) 11:40:14

Q. You have to say "yes" or "no", so 11:40:16

she can have an answer. 11:40:19

A. Yes. 11:40:20

Q. Or some audible response. Okay. 11:40:21

I think there we might have identified one of those typos and I just want to clarify that. 11:40:27 11:40:30 11:40:32

So the next sentence say: 11:40:32

"In performing my analysis and rendering my opinions, where the Board of Acqis ..." 11:40:34 11:40:36 11:40:38

-- I think that should be "or Acqis" but you tell me -- 11:40:39 11:40:43

"... has proposed a construction of the BRI of a claim term, I have applied that construction in my analysis." 11:40:44 11:40:59 11:40:49

Should that be "Board or Acqis"? 11:40:50

A. Well, for all the broadest reasonable interpretation cases and further I have referred to the Board. So in my understanding this is the Board for this Acqis case, and not written -- 11:41:01 11:41:02 11:41:04 11:41:06 11:41:07

Q. Oh, is that what you meant? Okay. It wasn't clear whether you meant the Board meaning like Board of Directors of Acqis or you meant Board of Patent Appeals or Acqis. So 11:41:10 11:41:13 11:41:15 11:41:17

what's your --   11:41:21
A.   No, I've referred, I mean, to what the Board has said in some of the cases which are discussed further, right? It's either the decision of the Board or what I would consider, as an expert in this field, to be the broadest reasonable interpretation.   11:41:22 11:41:27 11:41:29 11:41:34 11:41:36 11:41:41
Q.   But I believe there are some instances in which Acqis has proposed a broadest reasonable interpretation.   11:41:42 11:41:45 11:41:52
A.   Inside the patent, yes.   11:41:52
Q.   Correct. And you used Acqis's proposed broadest reasonable interpretation in a few instances as well, correct?   11:41:54 11:41:58 11:42:00
A.   If as set forth inside the patent documents, correct.   11:42:02 11:42:05
Q.   What patent documents are you talking about? Just so we're on the same page. Do you mean in the patents themselves?   11:42:06 11:42:09 11:42:11
A.   Yeah, as we refer here to the '814 then it would have to be the '814 document, you're right.   11:42:12 11:42:15 11:42:19
Q.   Okay, I just want to make sure I understand so we're clear for the record, because there's different patent documents: there's the   11:42:19 11:42:21 11:42:24

patent, there's the file history. Just so we're clear I may ask you to clarify what we're talking about, okay? 11:42:28 11:42:30 11:42:32

And then it says: 11:42:33

"Otherwise, I have interpreted claim terms by giving them the ordinary meaning that they would have to a [person of skill in the art], reading the '814 patent with its priority filing date (October 30, 1998) in mind, and in light of its specification and file history." 11:42:41 11:42:42 11:42:46 11:42:48 11:42:53 11:42:57

Do you see that? 11:43:03

A. I see that, yes. 11:43:03

Q. So just to be clear, if the Board gave an interpretation of what it found to be the broadest reasonable interpretation, you applied the Board's interpretation correct? 11:43:04 11:43:07 11:43:10 11:43:12

A. Correct. 11:43:14

Q. If you don't have a Board interpretation then you used the ordinary meaning of the term or the broadest reasonable interpretation of the remaining terms? 11:43:15 11:43:16 11:43:20 11:43:24

MR. DAVIS: Objection to form. 11:43:28

BY MR. BUROKER: 11:43:30

Q. Or do you think they mean the same thing? The ordinary meaning means the same thing 11:43:31 11:43:32

as broadest reasonable interpretation? 11:43:34
MR. DAVIS: Objection to form. 11:43:36
THE WITNESS: The broadest reasonable 11:43:40
interpretation in light of the specification. 11:43:45
This is what I used. 11:43:46
BY MR. BUROKER: 11:43:48
Q. So where it says "ordinary 11:43:48
meaning" what you meant is the broadest 11:43:49
reasonable interpretation in light of the 11:43:53
specification of the term? 11:43:53
A. It's my understanding this is what 11:43:56
I'm supposed to do. 11:43:57
Q. All right, it wasn't clear and 11:43:59
that's why I wanted to ask that question. 11:44:00
THE WITNESS: I would like to go to the 11:44:04
bathroom one more time. 11:44:06
MR. BUROKER: The bathroom again? 11:44:08
Sure. 11:44:09
THE WITNESS: Yes, it's almost 12:00 11:44:10
now. 11:44:12
MR. BUROKER: Yes, let's go off the 11:44:13
record. 11:44:14
(Brief recess taken 11:44 a.m. - 11:51 a.m.) 11:51:49
BY MR. BUROKER: 11:51:49
Q. So, turning then to paragraph 114. 11:51:53

MR. DAVIS: Just to be clear we're still on the '814. 11:52:04 11:52:05

MR. BUROKER: Yeah, I'm using that as the primary document. I know that they're very similar. 11:52:08 11:52:09 11:52:12

BY MR. BUROKER: 11:52:17

Q. So actually I was going to paragraph 113, sorry. 11:52:12 11:52:15

So in Section VII, "Claim Construction", you set forth your discussion of three terms that you specifically identified as providing construction for; is that correct? 11:52:17 11:52:21 11:52:29 11:52:37

A. Yeah, this is correct. 11:52:37

Q. And that's the "peripheral component interconnect (PCI) bus transaction" term, the "encoded" term and then the "extending from" term, correct? 11:52:39 11:52:41 11:52:42 11:52:45

A. This is correct. 11:52:46

Q. Okay. For the "PCI bus transaction" term, if I use that phrase you'll know which one I'm referring to rather than repeating the whole thing, right? So I'll just say "PCI bus transaction". 11:52:47 11:52:54 11:52:56 11:53:01 11:53:03

A. (The witness nodded.) 11:53:04

Q. Okay. So for the "PCI bus 11:53:06

transaction" term, you say that: 11:53:09

"... [the] Board construed the terms to mean 'Peripheral Component Interconnect ... industry standard bus transaction." 11:53:12 11:53:15 11:53:20

Correct? 11:53:21

A. Yeah. 11:53:22

Q. So that's the interpretation you used as the broadest reasonable interpretation? 11:53:22 11:53:24

A. Uh-huh, yes. 11:53:27

Q. But then you provide some additional thoughts on what that means in paragraph 114, right? 11:53:28 11:53:31 11:53:34

A. Yeah, it seemed important. 11:53:49

Q. Okay. So you say that a PCI bus transaction must include the PCI address and bus command information during the address phase and the PCI data byte enables during the data phase. Is that your understanding? 11:53:51 11:54:11 11:54:20 11:54:23 11:54:27

A. Amongst other things, yes. Although I just don't see it where I wrote this in detail. 11:54:30 11:54:32 11:54:37

Q. Well let me look for it, too. Oh here it is. So the second line on page 77 after the semicolon, you say: 11:54:38 11:54:54 11:54:56

"... they require the address and data 11:55:01

phases of a PCI bus transaction, which includes 11:55:03
the PCI address and bus command information 11:55:06
during the address phase ..." 11:55:09
And then you cite to the PCI spec and 11:55:11
then you say: 11:55:14
"... and the PCI data and byte enables 11:55:15
during the data phases." 11:55:17
Do you see that? 11:55:19
A. That is correct, yeah, yeah. 11:55:20
Q. When you say "they", you are 11:55:22
referring to the claims? You can read the whole 11:55:26
sentence but I'm trying to understand what you 11:55:30
mean when you say "they require". 11:55:32
A. In the claims discuss 11:55:40
communicating PCI transactions, so the claims do 11:55:42
not require the PCI bus transactions occur on 11:55:50
a PCI bus, they require the address and data 11:55:53
phases and so forth. So the "they" in this 11:55:56
context refers to the claims to make clear that 11:56:01
what PCI bus transaction really has to include. 11:56:06
Q. So is it your understanding that 11:56:14
you need to communicate the PCI address and bus 11:56:20
command information during an address phase and a 11:56:25
PCI data and byte enables during the data phase 11:56:28
to have communicated a PCI bus transaction? 11:56:33

A. Yes. If you would leave any of those out it cannot work. For example, if you leave the command out, the target being addressed wouldn't know where the read is or the write is or the configuration and so forth, that has to be there. And there is even more context which is set forth in the PCI specification, which has to be there for a PCI transaction to function. 11:56:37 11:56:41 11:56:45 11:56:49 11:56:51 11:56:55 11:56:59 11:57:03

Q. Okay. I'm just trying to understand. That's the understanding of the term "PCI bus transaction" that you used in analyzing the claims as compared to the prior art that was asserted in these IPRs, correct? 11:57:07 11:57:08 11:57:15 11:57:20 11:57:23

A. Yeah. 11:57:27

Q. So let's look at the claims. So that's the '814 patent which is the 1001 from the '1469 IPR. And then I'll give you the '873 Patent which is 1001 from the '1462 IPR. 11:57:27 11:57:45 11:57:55 11:58:01

THE WITNESS: Oops they have the same reference number. 11:58:09 11:58:11

BY MR. BUROKER: 11:58:11

Q. Right, they do, because of the weird way in which the PTO PTAB procedures require that we number exhibits. So rather than use the exhibit number, if we just talk about 11:58:12 11:58:13 11:58:15 11:58:19

which patent you're looking at. 11:58:21

So looking at the '814 Patent, claim 24, let's start down with the element that says, "a second LVDS channel". Do you see that one? It's the sixth or seventh one down. 11:58:24 11:58:45 11:58:52 11:58:55

A. Yeah. 11:58:55

Q. Okay, so one of the elements of the claim talks about: 11:58:59 11:58:59

"A second LVDS channel comprising two unidirectional serial channels that transmit data in opposite directions, said second LVDS channel extending from said north bridge ..." 11:59:00 11:59:05 11:59:07 11:59:13

-- and it says: 11:59:16

"... to convey said address and data bits of PCI bus transaction in serial form." 11:59:16 11:59:20

Do you see that? 11:59:25

A. I see that. 11:59:29

Q. And then up in the northbridge limitation, a couple of limitations up, it says: 11:59:29 11:59:31

"A north bridge to communicate address and data bits of PCI bus transaction in serial form ..." 11:59:33 11:59:36 11:59:40

Do you see that? 11:59:40

A. Ah, here we are, yes. 11:59:46

Q. Okay. So in both of those 11:59:49

limitations there's this phrase "address and data bits of PCI bus transaction in serial form". 11:59:51 11:59:55

A. Uh-huh. 12:00:01

Q. Right? 12:00:02

A. Yes. 12:00:02

Q. So you agree that that phrase uses the singular form of the word "transaction", correct? 12:00:03 12:00:10 12:00:14

A. Yes. 12:00:24

Q. So it doesn't say "transactions", it just says "transaction", correct? 12:00:25 12:00:27

A. It says that, yeah. 12:00:31

Q. Okay. So that would cover a situation in which a single transaction is communicated, right? 12:00:32 12:00:36 12:00:42

A. Well, I mean, in any particular case only one PCI transaction can occur at any point in time. It's a bus. 12:00:45 12:00:47 12:00:51

Q. But the claim doesn't require that the northbridge communicate multiple bus transactions, it just has to, at any point in time, communicate one to meet this claim, right? 12:00:54 12:00:56 12:01:01 12:01:04

MR. DAVIS: Objection to form. 12:01:08

THE WITNESS: The PCI specification lays out how a PCI transaction has to work, and 12:01:10 12:01:14

according to the specification at any point in time there is one PCI transaction ongoing on the bus. 12:01:19 12:01:21 12:01:23

BY MR. BUROKER: 12:01:24

Q. Right, and I'm asking you a question more about how you read these claims. So claim 24 is a method claim. It's your understanding that a method claim understands multiple steps that are performed, right? 12:01:25 12:01:26 12:01:28 12:01:34 12:01:36

A. Uh-huh. 12:01:38

Q. Okay. And one of those steps is inserting an attached computer module into the bay of a console and then the rest of this claim -- not the rest but a lot of the other elements then specify what is inside the ACM, the attached computer module, right? 12:01:38 12:01:48 12:01:52 12:01:56 12:01:58 12:02:04

A. Uh-huh. 12:02:05

Q. And that's, you know, the microprocessor, northbridge, main memory and second LVDS channel are part of the ACM. Is that the right way you read this claim? 12:02:06 12:02:08 12:02:11 12:02:16

MR. DAVIS: Objection to form. 12:02:18

THE WITNESS: "Modular computing system, the console comprising a first ... LVDS signal -- differential signal channel comprising

two unidirectional serial channels that transmit encoded data of ... PCI -- Component Interconnect bus transaction in opposite directions."

Yes, this is what it says. It goes on: 12:02:41

"A microprocessor unit coupled to a 12:02:41
mass memory storage device; 12:02:41

A north bridge to communicate address 12:02:47
and data bits." 12:02:48

This is the claim. 12:02:49

BY MR. BUROKER: 12:02:49

Q. Right. But the way this claim is 12:02:52
structured, just so we are on the same page, is 12:02:54
that the microprocessor, northbridge, main memory 12:02:56
and second LVDS channel are defined what has to 12:03:00
be part of the ACM, correct? 12:03:07

MR. DAVIS: Objection to form. 12:03:10

THE WITNESS: The ACM comprises 12:03:13
a microprocessor coupled to a mass storage 12:03:16
device, the northbridge, communicating the data 12:03:18
bits in serial form, comprises a main memory, 12:03:22
coupled to the microprocessor unit through the 12:03:27
northbridge and the second LVDS channel. Yeah. 12:03:30

BY MR. BUROKER: 12:03:30

Q. Right, okay. So the northbridge 12:03:34
part of the ACM has to communicate address and 12:03:41

data bits of PCI bus transaction in serial form, 12:03:47
right? 12:03:51

A. Yeah. 12:03:54

Q. It doesn't say that it has to 12:03:54
communicate multiple PCI bus transactions in 12:03:56
serial form, it can but it doesn't have to do 12:03:59
multiple ones. Is that your understanding of how 12:04:03
to read this claim? 12:04:05

A. I don't understand the 12:04:08
differentiation you're trying to make here. If 12:04:09
the northbridge is capable of performing a PCI 12:04:16
transaction, a PCI is a defined standard. In 12:04:19
order to be compliant with that standard it has 12:04:24
to be capable of performing all the functionality 12:04:28
set forth by the standard or it would be 12:04:30
incompatible and it would not be allowed to use 12:04:32
the term. So that means, of course, one cannot 12:04:35
limit this claim to saying if there is one single 12:04:38
particular PCI transaction executed or capable of 12:04:41
-- if the northbridge is capable of doing just 12:04:46
one particular transaction and not the features 12:04:48
as defined by PCI, that would not be a correct 12:04:54
interpretation. So this is why I'm a little 12:04:59
confused why you're trying to disentangle between 12:05:01
singular and plural here. 12:05:04

Q. So that's the way you read this northbridge limitation, the way you've just explained it then? 12:05:07 12:05:08 12:05:11

A. (The witness nodded.) 12:05:13

Q. Okay. Now, the claim says that you have to communicate address and data bits. You would agree with me that it doesn't mention command information, correct? 12:05:14 12:05:17 12:05:22 12:05:25

MR. DAVIS: Objection to form. 12:05:28

THE WITNESS: It says: 12:05:31

"... address and data bits of PCI transaction in serial form ..." 12:05:34 12:05:37

It doesn't say explicitly the other corollary information which is needed to define a PCI transaction, but it says "PCI transaction". So without, for instance, the additional functionality, it wouldn't be a PCI transaction. 12:05:38 12:05:41 12:05:44 12:05:48 12:05:55

BY MR. BUROKER: 12:06:10

Q. So even though the word "command information" is not expressly present, it's your reading of this claim that the northbridge must communicate PCI bus command information in serial form as well; is that correct? 12:06:10 12:06:12 12:06:15 12:06:20 12:06:24

A. If you read this patent you will find that this context is defined as such. It is 12:06:28 12:06:30

about a PCI transaction. 12:06:34
Q. Okay. The claim also doesn't 12:06:35
expressly require transmission or communication 12:06:40
of what you call byte enables either, does it? 12:06:43
A. It doesn't explicitly state, yes. 12:06:49
Q. But, again, it's your 12:06:52
understanding that to meet this claim the 12:06:53
northbridge must communicate byte enables from 12:06:57
a PCI bus transaction, correct? 12:07:03
MR. DAVIS: Objection; form. 12:07:05
THE WITNESS: There is signals on the 12:07:08
PCI bus, data bus signals, which are invalid 12:07:10
because of byte enables being set to invalid. So 12:07:14
this has to be encoded in some form, otherwise 12:07:20
the data, again, has no meaning. 12:07:23
BY MR. BUROKER: 12:07:27
Q. And the phrasing here also doesn't 12:07:28
say that you have to communicate all of the 12:07:32
address and data bits of a PCI bus transaction. 12:07:36
Do you agree? 12:07:41
A. It doesn't explicitly say that, 12:07:43
but, again, if I give you a telephone number but 12:07:47
leave out two digits, what relevance does it 12:07:53
have? 12:07:58
Q. Right. So, in your view, if the 12:08:00

northbridge did not communicate all of the 12:08:04
address and data bits and all of the command 12:08:07
information and byte enables of a PCI bus 12:08:09
transaction in serial form, you would believe 12:08:14
that that northbridge doesn't meet this claim 12:08:17
limitation; is that correct? 12:08:20

A. It wouldn't be a PCI bus 12:08:21
transaction. 12:08:23

Q. Well, the question is: if the 12:08:23
northbridge didn't communicate all of the address 12:08:26
and data bits and all of the bus command 12:08:30
information and byte enables but only 12:08:33
communicated some of those bits, in your view it 12:08:36
wouldn't meet this claim's requirement, right? 12:08:39

A. I believe that's correct, yeah. 12:08:43

Q. And you say you're getting that 12:08:45
from reading the specification. Do you cite 12:08:51
anywhere in this explanation where the 12:08:59
specification dictates that or is it from the PCI 12:09:01
specification alone? Let me strike that because 12:09:06
the word "specification" is confusing. 12:09:10

Are you getting that from the 12:09:12
requirements of the PCI specification or the 12:09:14
patent specification or both? 12:09:17

MR. DAVIS: Objection; form. 12:09:22

THE WITNESS: First, this is in the context of a PCI bus transaction and this is well defined, if you leave something out, remove something, then it is not, again, according to the specification, it wouldn't function and also looking at the problem the patent solves would require this information to be there. 12:09:25 12:09:27 12:09:31 12:09:33 12:09:37 12:09:43 12:09:48

BY MR. BUROKER: 12:09:50

Q. Okay, let me give you then, just in case you need it, the ... 12:09:51 12:09:52

A. The PCI local bus specification 2.1. 12:09:58 12:09:58

BY MR. BUROKER: 12:10:00

Q. This is Exhibit 2001, I'm not sure if it's in both or which of the -- it's 2001 in one of the two IPR proceedings. 12:10:00 12:10:03 12:10:08

MR. DAVIS: I think it's in both, but I'm not positive on that. 12:10:10 12:10:12

BY MR. BUROKER: 12:10:14

Q. Okay, I think so too. 12:10:15

But anyway you've seen this before obviously. 12:10:16 12:10:21

A. Yeah. 12:10:22

Q. Okay. And this is PCI Spec Rev 2.1 that's referred to in your declaration 12:10:22 12:10:26

paragraph 114; is that right? 12:10:29

A. 114 I have to verify but, yes, it's certainly being referenced. 12:10:33 12:10:36

Q. Sorry, you have multiple documents open at once. Do you have that? 12:10:36 12:10:36

A. Yeah. And I believe there is some language about what is the correct version of the PCI local bus specification because this thing has been a little bit iterative. The 2.2 I believe was followed around '99/2000, I don't remember exactly. Although the changes, the differences between 2.1 and 2.2 are minor and not relevant here, but just to be correct. I think it's on page 30. 12:10:45 12:10:49 12:10:52 12:10:58 12:11:03 12:11:06 12:11:09 12:11:12 12:11:15

Q. And so you're -- oh, go ahead, you're still answering. 12:11:22 12:11:25

A. 2.1 is the relevant one being valid at the time. 12:11:42 12:11:46

Q. Right. So in paragraph 114 you cite to page 30 of this PCI specification Exhibit 2001. So can you point me to which particular portion of page 32 you were -- 12:11:47 12:11:49 12:12:00 12:12:06

A. 30 or 32? 12:12:09

Q. It says 32 in your declaration. 12:12:10

A. I'm just trying to find the 12:12:43

context so it is clear. 12:12:44
Q. And if it's meant to be 12:12:46
a different page we can correct it, that's one of 12:12:47
the reasons I asked that question. I'm not sure 12:12:49
that that's -- anyway, I'll let you testify. 12:12:50
My question is which portion of the PCI 12:12:52
Spec Revision 2.1 supports your view that the 12:12:54
claims require the address and data phases of the 12:13:01
PCI bus transaction which include the PCI address 12:13:05
and bus command information during the address 12:13:07
phase and the PCI data and byte enables during 12:13:10
the data phases? 12:13:13
A. I mean these references are meant 12:13:15
to be examples in any case because when we're 12:13:16
talking about a PCI, then this is what it is, 12:13:21
right? Like, with every interface document or 12:13:23
standard -- this is a de facto standard -- if you 12:13:29
violate parts of it you don't have a standard 12:13:34
anymore and it doesn't work anymore because the 12:13:37
reason for this is to enable different devices to 12:13:39
communicate. 12:13:42
Now, this reference here is about the 12:13:43
requirement that there is address and command 12:13:44
information during the address phase at 32. So 12:13:47
let me just see, this is a long page of text it 12:13:51

must be in here. Let me look this up. 12:13:54
No, this is all transaction language. 12:14:27
I can't find it right now. Which is really 12:14:54
strange because we went over the references to be 12:14:57
correct, quite a few times. 12:15:02
Q. I just double checked, you also 12:15:10
cite the page 32 in the declaration for the '873 12:15:13
Patent. 12:15:18
A. Then it would be just consistent. 12:15:18
Q. So that's why if you need to take 12:15:21
your time to find it, you know, I wanted to make 12:15:24
sure we understood what you're referring to when 12:15:27
you cite to the address and bus command 12:15:32
information during the address phase and the PCI 12:15:40
data and byte enables during the data phase. So 12:15:45
if you need to take time to -- 12:15:48
A. I mean I found a few places where 12:15:48
that is already quite obvious, but now I'm trying 12:15:50
to see anywhere near page 32 because the 12:15:53
references should be right. 12:16:01
This is all about transaction ordering 12:16:46
which is at a higher level of bus protocol. 12:16:48
I would like to review this but I can give you 12:17:00
here another example where this is very clearly 12:17:05
stated, so that you have it. 12:17:09

Q. Where are you looking at? 12:17:10
A. It may not be the best example for 12:17:12
a citation. Page 36, which is an example of 12:17:13
a read transaction, 37 a write transaction. And 12:17:19
there you see basically the major required 12:17:26
functionality and signals referring to 12:17:30
Figure 3-1, Basic Read Operation. A PCI 12:17:40
transaction is always initiated by the first 12:17:43
clock state with frame being low, the upper 12:17:47
signal trace. And I should say PCI is what is 12:17:52
called a synchronous bus, all signals are with -- 12:17:55
Q. Can you say that again? I didn't 12:17:58
understand it. A what? 12:17:59
A. Synchronous bus. 12:18:04
Q. Synchronous bus, okay. My 12:18:06
apologies, you said it just fine, I just couldn't 12:18:06
pick it up. A synchronous bus, okay. 12:18:08
A. As compared to an asynchronous bus 12:18:10
which is VME. 12:18:15
That means basically only the signal 12:18:15
level -- we like to call it state -- at the 12:18:19
rising edge of the clock signal is relevant; 12:18:21
anything in between doesn't matter. Which means 12:18:25
you can basically take the bus state wherever 12:18:28
these dashed lines are or dotted lines are, the 12:18:32

vertical lines, and say this is a state. So 12:18:35
state number 1, clock number 2, frame low, always 12:18:39
defines the beginning of the transaction. And 12:18:44
the first clock of every PCI transaction has to 12:18:47
be the address and command. And you see that 12:18:51
with "AD" labeled as "address". PCI is to save 12:18:54
pins, what is called a multiplexed address data 12:19:02
bus, meaning it uses the same signal pins for 12:19:07
address and data information, depending on the 12:19:11
state of the bus. So, basically -- and, I mean, 12:19:14
this is obvious to do it like that, the first 12:19:18
clock says, "What does the master want to do and 12:19:21
where? Where is the address? What is the 12:19:25
command?" 12:19:27

I will skip the initiator and target 12:19:29
ready signals because they're only for flow 12:19:33
control. 12:19:35

The device selected signal is there to 12:19:36
enable the selected device to say, "I'm there". 12:19:38
The reason being it may take a long time for 12:19:46
a device to answer and the bus master has to be 12:19:48
able to disentangle the slow device from a not 12:19:52
existing device, which is important in case of 12:19:57
the automatic configuration functionality, these 12:19:58
whole configuration cycles. 12:20:02

The bus commands are nicely outlined, and this figure I even posted in my deposition. It's -- now, where are we -- also here in the specification, of course, which is page -- I just saw it. Here we are, page 21, right? It's a 4-bit field, so you have 16 commands, all 16, or mostly all 16 are defined, which gives you the set of transactions available. 12:20:03 12:20:05 12:20:13 12:20:16 12:20:29 12:20:37 12:20:43 12:20:49

After the address phase, as it's been called, there is an arbitrary number of data phases, the length is only limited by some environmental configuration, which is not specified here, a PCI transaction must not exceed a certain length so that nobody can block the bus for too long. And then every time target and initiator simultaneously say "I'm ready", data is exchanged, as you can see from this diagram. 12:20:52 12:20:55 12:20:59 12:21:03 12:21:06 12:21:09 12:21:12 12:21:16 12:21:20

And that is valid for basically every transaction although they have different meanings and different flavors. So a configuration transaction still would have the appropriate command byte enables but a couple of details would be different. And, for instance, if there is a read multiple, these cache line type transactions, then there is an indication as to 12:21:22 12:21:25 12:21:27 12:21:30 12:21:32 12:21:35 12:21:39 12:21:43

how many words are exchanged and so forth. 12:21:45
But this is basically the context which 12:21:47
needs to be there for a PCI transaction to be 12:21:52
complete. Write transaction is same thing, 12:21:54
except -- and this is why these are different 12:21:57
diagrams -- the data flow is different. We can 12:21:59
see nicely from Figure 3-2 that the address phase 12:22:01
is immediately followed by a data phase, which is 12:22:07
obviously making sense because if somebody wants 12:22:10
to write, this is then the master. The 12:22:13
initiator, as it's called in PCI, would have to 12:22:15
have the data to write otherwise it wouldn't want 12:22:18
to write, so it can submit the data immediately 12:22:20
on to the bus. 12:22:23
In case of a read transaction, the 12:22:24
target would have to notice, "Ah, I'm the one 12:22:26
being addressed", but then it has to access its 12:22:30
local resources to find that data to respond to 12:22:33
which is obviously not going to happen within a 12:22:36
clock. It cannot be. And there is an additional 12:22:39
requirement, there is a minimum of one clock 12:22:42
which is shown by these nice little arrows here, 12:22:44
which is called a bus turnaround cycle, because 12:22:47
here we have first the master driving the bus, 12:22:49
then data comes back to the master, so the master 12:22:52

has to release the bus, and the slave, the 12:22:55
responding device, has to drive the data signals 12:22:57
now. And in order to avoid race conditions where 12:23:00
both drive simultaneously, which is electrically 12:23:05
really bad, basically a short circuit, there is 12:23:10
this turnaround cycle. 12:23:11

Q. Okay, yeah, that was a lot of 12:23:15
testimony there, so just so we break it down 12:23:16
a little bit. 12:23:19

So you get the idea that you have to 12:23:19
have address and data phase and the address phase 12:23:21
has to include the address and bus command and 12:23:28
the data phase has to include the data and byte 12:23:31
enables from reading the specification as 12:23:32
a whole, in particular looking at the command 12:23:36
definitions, and then the explanation of how each 12:23:41
transaction works in this specification, right? 12:23:44

A. Yeah, and I think we should 12:23:46
probably see whether we can find a nicer 12:23:48
reference here because I couldn't find it, or if 12:23:51
I overlooked something I can point you to it 12:23:56
tomorrow. 12:23:58

Q. It's more of a summary rather than 12:23:58
a whole bunch of pages to read through? 12:24:00

A. Yeah, but, again, it's a standard. 12:24:02

So unfortunately these standards tend to be long 12:24:07
and bulky. 12:24:10
Q. So let me ask you something else 12:24:11
about what you did when you were looking at this. 12:24:13
If the northbridge is able to send this 12:24:17
information about any of these transactions, you 12:24:22
said there were 16, is that all that's necessary 12:24:26
in your mind or does this claim require that the 12:24:29
northbridge be able to communicate the address 12:24:33
and data phases of all of the different types of 12:24:37
PCI bus transactions laid out in this PCI 12:24:40
specification? 12:24:42
A. And which part of the document are 12:24:45
we now looking at, just to be clear? 12:24:47
Q. Which document? The declaration? 12:24:49
Same paragraph, 114, you say: 12:24:52
"[The claims] require the address and 12:24:55
data phases of a PCI bus transaction." 12:24:58
So can that be any of the 16 PCI bus 12:25:02
transactions or does it require that you be able 12:25:06
to do that for all 16? 12:25:08
A. Yes. For example -- 12:25:11
Q. So that what -- 12:25:15
A. -- if you do away with the PCI 12:25:17
configuration you will never get to a normal 12:25:19

memory read or write because you can't configure the system and it's useless. So you have to be able to -- a few of them are optional, but those required -- and these are configuration I/O on memory read and write -- they have to be there for the system to function. 12:25:24 12:25:26 12:25:30 12:25:34 12:25:38 12:25:41

Q. So which ones are mandatory? 12:25:43

A. Certainly configuration, memory read and write. I believe also I/O. It's stated in here somewhere. I believe that dual address cycle is optional and only required in systems which do 64-bit addressing in a 32-bit system. Most of them are required. 12:25:50 12:25:53 12:25:57 12:26:17 12:26:07 12:26:13

Q. Memory read and memory write required, right? 12:26:18 12:26:20

A. Certainly. 12:26:21

Q. And then you say configuration read and configuration read are required? 12:26:22 12:26:24

A. Absolutely essential. These are the first transactions ever done in PCI, otherwise it won't work. 12:26:27 12:26:29 12:26:31

Q. What about the very first one, interrupt acknowledge? 12:26:32 12:26:35

A. An I/O, an external device without interrupt, will require the CPU to pull the 12:26:39 12:26:43

device, which is highly inefficient, so required.

Q. Yes, what's special cycle?

A. That I'm not sure at the moment. Let me have a quick look. Possibly required, possibly not; that I don't know off the top of my head. There is a list of transactions being outlined in here and this should also say. I don't remember ever using it, 372, I've designed so many pieces to play with myself. This is a broadcast command. It doesn't say that it is optional, so it is required. At least I don't see that it claims it to be optional.

Q. And then there's a bunch of reserved ones. But then you skip down to 1100 memory read multiple, is that required or optional?

A. It's not saying optional, so it's mandatory.

Q. And then you say dual address cycle is optional; is that correct?

A. I believe so. Let me just verify:

"... is used to transfer 64-bit address to devices that support 64-bit addressing when the address is not in the low 4 [gigabyte] address space. Targets that support only 32-bit

addresses must treat this command as reserved and not respond to the current transaction in any way." 12:29:02 12:29:05 12:29:08

So this is kind of a hybrid of mandatory; it doesn't have to be supported but then there is a defined reaction to it. 12:29:09 12:29:12 12:29:16

Q. And then the next memory read line, is that optional or mandatory? 12:29:19 12:29:22

A. It doesn't say optional so it's required. 12:29:36 12:29:38

Q. And then finally memory write and invalidate? 12:29:38 12:29:45

A. This is both. Cache semantics; both don't say it is optional, so mandatory. So basically most of it is mandatory, as I expected. 12:29:47 12:29:55 12:29:59

Q. So, go back to claim 24, there's a different, slightly different phrase earlier in the claim in the inserting step, it says that the: 12:30:03 12:30:19 12:30:23 12:30:23

"... unidirectional serial channels that transmit encoded data of Peripheral Component Interconnect (PCI) bus transactions in opposite directions ..." 12:30:31 12:30:34 12:30:39 12:30:43

Is it your understanding and the understanding that you applied in your analysis 12:30:48 12:30:50

of encoded data of peripheral component 12:30:52
interconnection bus transaction means an encoded 12:30:57
PCI bus transaction that includes the address and 12:31:03
data phases which includes the PCI address and 12:31:05
bus command information during the address phase 12:31:09
and the PCI data and byte enables during the data 12:31:11
phase? 12:31:15

MR. DAVIS: Objection; form. 12:31:16

THE WITNESS: You're referring to 12:31:29
saying is the word "data" to be interpreted in 12:31:31
the strictest sense of it just being data or data 12:31:35
in the sense of everything containing the 12:31:38
transaction? Did I understand the question 12:31:42
correctly? 12:31:46

BY MR. BUROKER: 12:31:47

Q. Well, right, is there a difference 12:31:47
in your mind in terms of your analysis between 12:31:49
data of PCI bus transaction versus, later in the 12:31:53
claim, address and data bits of PCI bus 12:31:58
transaction? 12:32:03

MR. DAVIS: Objection; form. 12:32:04

THE WITNESS: I notice that there is 12:32:08
a certain amount of redundancy in these claims. 12:32:09
Here I would say it means the encoded data as 12:32:16
data phases of the PCI transaction, but later 12:32:22

it's more detailed further in to include the addresses as well. 12:32:25 12:32:35

BY MR. BUROKER: 12:32:38

Q. Right, so you would read the "data" here as referring only to the data phase of the PCI bus transaction? 12:32:38 12:32:45 12:32:49

A. I would say so. Yes. 12:33:02

Q. Okay, and is that because the word "address", is not explicitly included? 12:33:05 12:33:07

A. Yes. 12:33:12

Q. Okay. But earlier the command information was not explicitly included in the phrase "address and data bits of PCI bus transaction" and I think you said that you had to transmit the command information done in that claim; is that correct? 12:33:12 12:33:18 12:33:21 12:33:24 12:33:28 12:33:31

A. I remember that. For it to make sense it has to include that, yeah. 12:33:32 12:33:34

Q. And so in the first instance for it to make sense you don't have to send the address information or the command information in the "transmit encoded data of PCI bus transaction" clause? 12:33:37 12:33:40 12:33:42 12:33:47 12:33:52

A. I notice you're trying to construct a contradiction here, yeah. 12:33:54 12:33:56

Q. I'm not trying to do anything, I'm asking you questions. It's your understanding that you applied in your analysis. 12:33:58 12:34:00 12:34:06
A. Let me just ... 12:34:14
MR. DAVIS: I object to form on the last question. 12:34:25 12:34:26
THE WITNESS: Well one claim says "address and data bits of PCI bus transaction" but always referring to PCI bus transactions and up here it says "data of PCI bus transaction", it says "encoded data". 12:34:29 12:34:40 12:34:44 12:34:48 12:34:58
BY MR. BUROKER: 12:35:12
Q. So let me just make it a simpler question. As you applied claim 24, what did you understand the phrase "data of PCI bus transaction" to be? 12:35:12 12:35:14 12:35:23 12:35:27
A. I always saw this in the context of the PCI transaction, bus transaction. 12:35:32 12:35:34
Q. Meaning that it was the data phase of the PCI bus transaction? 12:35:38 12:35:39
A. Yeah. Let me rethink this. Because in both cases, whether we are talking about the lower part of the claim or the upper part of the claim, there has to be the PCI transaction information in there otherwise this 12:35:47 12:36:06 12:36:09 12:36:11 12:36:16

sentence wouldn't make much sense. 12:36:22

Q. So there are other asserted 12:36:25
claims, so claim 31 of the same patent doesn't 12:36:29
have the "encoded data" language, but it does 12:36:36
have the "address and data bits of PCI bus 12:36:40
transaction in serial form". Do you see that? 12:36:43

A. Yeah. 12:36:45

Q. Okay. And then claim 54 of the 12:36:46
'873 Patent -- which is the other asserted claim, 12:36:51
that's the other one you've got there -- in the 12:36:54
low voltage differential signal channel element 12:37:09
it uses the phrase: 12:37:13

"... communicating an encoded serial 12:37:18
bit stream of ... PCI bus transaction." 12:37:21

Do you see that? 12:37:23

A. Yes. 12:37:24

Q. Okay. So, what do you understand 12:37:25
the serial bit stream of PCI bus transaction to 12:37:30
be? And which interpretation did you apply in 12:37:33
your analysis? 12:37:39

A. We're referring to a PCI bus 12:37:49
transaction, so the information which PCI bus 12:37:53
transaction is ongoing, what state it is at any 12:37:58
particular time has to be conveyed, and it is 12:38:01
being encoded and submitted as a serial bit 12:38:03

stream. So, whatever constitutes to a PCI bus transaction, the relevant signals -- and we went through it -- would have to be encoded in serial form. 12:38:07 12:38:13 12:38:18 12:38:24

Q. So the whole PCI bus transaction including any command information or byte enables, including the address and data, that whole thing would have to be encoded in serial form? 12:38:25 12:38:29 12:38:35 12:38:37 12:38:42

A. Yes. 12:38:45

MR. BUROKER: Why don't we take a break for lunch? 12:39:08 12:39:09

(Lunch recess taken 12:39 p.m. - 1:26 p.m.) 12:39:10

BY MR. BUROKER: 01:26:31

Q. Welcome back. I should have said this at the beginning, but you did not talk about the substance of your testimony with your counsel at the lunch break, did you? 01:26:32 01:26:36 01:26:38 01:26:41

A. (The witness shook his head.) 01:26:44

Q. Yeah, great. That was a "no", correct? 01:26:44 01:26:45

A. This is an affirmative. 01:26:46

Q. That you did not? 01:26:49

A. I did not. 01:26:52

Q. I apologize for the negative 01:26:53

question. 01:26:55
A. That's fine, don't worry. I did 01:26:56
not think I should. 01:26:58
Q. I have a question going back to 01:26:59
the PCI specification document. You were looking 01:27:02
I believe at page 36 at the read transaction as 01:27:04
an example of a transaction. 01:27:06
MR. DAVIS: Are you pointing at page 36 01:27:21
of the document? 01:27:23
MR. BUROKER: Oh, I'm sorry 36 of the 01:27:25
document, which is page 52 of the exhibit. It's 01:27:27
the 3.3.1 Read Transaction section. 01:27:30
A. Okay, this the one. 01:27:56
Q. Okay, so we were looking at this 01:27:58
earlier this morning, correct? 01:28:01
A. Yes. 01:28:02
Q. Are some of the elements along the 01:28:10
left-hand side called control lines in the PCI 01:28:11
specification? 01:28:14
A. I would consider them as such, 01:28:21
whether they are explicitly called control 01:28:23
signals I would have to check. But basically in 01:28:26
bus terminology you have the address, the data 01:28:33
and then additional corollary signals which 01:28:38
basically define what's going on, right? And 01:28:42

those constitute, in this case, the combined byte 01:28:44
enables, then the initiator ready, target 01:28:49
ready -- IRDY and TRDY -- which are basically 01:28:53
used for the flow control, and the device select 01:28:58
which is used for enabling the device to claim 01:29:01
its existence in the bus. 01:29:04

Q. What is the "frame#" what is that? 01:29:05

A. And frame, of course, excuse me. 01:29:09
The frame. The frame signal is there to define 01:29:10
the length of the transaction. This is a very 01:29:14
fundamental thing because, unlike in other cases, 01:29:17
in particular typically in networks, where the 01:29:21
length of the packet is basically submitted as 01:29:24
one of the very first words in the head of the 01:29:27
packet saying, "This is it" and, "This is how 01:29:29
long it will be." In PCI this doesn't exist. So 01:29:31
a target being connected has no way of knowing 01:29:35
how long this transaction will end up being, 01:29:37
right? It will only know here is an address and 01:29:41
here is a command, what is going to happen? And 01:29:44
the length of the transaction is determined by 01:29:46
the length the frame signal is asserted and if 01:29:48
you refer, for instance, to column 8, clock cycle 01:29:52
8, you see that there is one last data transfer 01:29:56
when frame is already high. This is basically 01:30:00

an efficiency thing which says since you have to 01:30:03
de-assert, make invalid the frame signal at the 01:30:09
end of the cycle to enable the next cycle, the 01:30:12
idea was to use that mandatory state for another 01:30:17
data phase in order not to have a dead state in 01:30:22
the bus protocol. 01:30:25

Q. Okay. So in a PCI bus are there 01:30:26
separate lines for frame number, IRDY, TRDY, 01:30:37
DEVSEL? 01:30:48

A. Yes. 01:30:48

Q. Okay. So of the 37 lines of a PCI 01:30:49
bus, those take up five of the bits; is that 01:30:53
correct? Or five of the lines I'm sorry. 01:31:01

A. If the sum is 37, I'm not 01:31:03
100 percent sure. But if you refer to Figure 2-1 01:31:05
on page 7 of the same document they are nicely 01:31:08
outlined. So, for example, one signal which is 01:31:11
also always part of the game which is not shown 01:31:11
here -- 01:31:11

Q. Sorry, did you say Figure 2-1? 01:31:11

A. Figure 2-1. The PCI pin list. 01:31:11

Q. Which page is that on? 01:31:31

A. Page 7 or 23. 01:31:31

So there is also the parity signal which 01:31:36
is used for signal integrity and then you see 01:31:38

here it's called the control signals, frame, target ready, initiator ready. There is in addition the stop signal which is not disclosed in this diagram, which enables a device to say, "Terminate the transaction, no point going further, illegal address", something like that. So there are other transactions showing that in this spec and then device select and ID select. 01:31:41 01:31:47 01:31:53 01:31:55 01:31:59 01:32:01 01:32:04 01:32:08

Q. Yeah, I said 37 but I think it says at the top of page 7, 47 pins not 37, right? 01:32:14 01:32:16

"The PCI interface requires a minimum of 47 pins for a target-only device and 49 pins for a master to handle data in addressing, interface control, arbitration and system functions." 01:32:18 01:32:20 01:32:24 01:32:28 01:32:30

Correct? 01:32:31

A. 37 seemed a bit low to me, yeah. 01:32:31

Q. Do these control lines, such as frame, target ready, and so forth, are they part of the PCI bus transaction as you understand that term in the claims of the patent? 01:32:35 01:32:42 01:32:47 01:32:50

MR. DAVIS: Objection; form. 01:32:58

BY MR. BUROKER: 01:32:59

Q. So, you know, earlier we were talking about what your understanding of the term 01:32:59 01:33:00

"PCI bus transaction", looking at paragraph 114, for example, of your declaration, and you stated claims require address and data phases of a PCI bus transaction, et cetera. Are these control lines also part of what the claims require as a PCI bus transaction?

A. Since they are required to define what is going on on the bus at any point in time, the answer is yes. They define the PCI transaction. If you, for example, would remove from one byte enable you have no way of knowing whether we are reading, writing, or what other functionality is to be executed. If you remove any of the flow control signals, you cannot steer the fact if a device is not immediately ready, which happens a lot. So they would have to be -- they define the transaction, so have to be there.

Q. Okay. Looking at claim 24 as an example again.

A. Just wait, wait, wait. And we are talking now '873?

Q. No, '814 Patent, claim 24.

The complete phrase that we were looking at talks about communicating address and data bits of PCI bus transaction in serial form. Do

you see that? 01:34:49
A. Yes. 01:34:49
Q. PCI bus transactions are not naturally in a serial form, correct? 01:34:54 01:34:56
A. They are not defined in a serial form in this document, correct. 01:34:58 01:34:59
Q. So if you take the transaction and transform it into a serial format, is the result still a PCI bus transaction? 01:35:10 01:35:13 01:35:16
MR. DAVIS: Objection; form. 01:35:20
(Brief pause to re-establish realtime connections.) 01:38:22
BY MR. BUROKER: 01:38:22
Q. Since we had a little bit of a technical issue, I'll just ask a new question. 01:38:23 01:38:24
The phrase is: 01:38:27
"... to communicate ... [the] PCI bus transaction in serial form ..." 01:38:28 01:38:31
What does it mean to you to communicate a PCI bus transaction in serial form? 01:38:35 01:38:38
MR. DAVIS: Objection; form. 01:38:42
BY MR. BUROKER: 01:38:46
Q. Well in actual fact let me ask a different question. 01:38:47 01:38:49
So the full language, and I'll give it to you, is: 01:38:49 01:38:51

"... to communicate address and data 01:38:52
bits of PCI bus transaction in serial form ..." 01:38:54
What does the phrase "in serial form" 01:38:56
in that phrase mean? 01:39:01
A. I mean, I defined even in 01:39:04
particular this serial transmission here, and, 01:39:08
let me just see, '814, there were a few terms 01:39:18
which I believe have been defined, now I just 01:39:21
have to see that I find it real quick, serial 01:39:24
communication, page 28 of this document. And 01:39:27
although I am quite sure I remember off the top 01:39:33
of my head, I'd rather refer to it. We say here: 01:39:39
"Serial communication protocols ..." 01:39:44
-- and I was instructed to speak really 01:39:48
slow when I read because I was not doing this -- 01:39:50
"... send bits of information one after 01:39:53
another on one or more lines that are used to 01:39:54
make up words. A communication scheme is said to 01:39:57
be serial if the information sent over the serial 01:40:05
lines has more bits in a word than there are 01:40:07
physical lines to transmit those bits." 01:40:10
And then there is more details, but I 01:40:12
think this is maybe already good enough for this. 01:40:15
So that means the information defining 01:40:19
a PCI transaction is sent over a number of 01:40:23

signals which are obviously less than what we have here. The corollary to that technically would mean it would have to be at a higher rate in order to keep up. 01:40:28 01:40:32 01:40:37 01:40:40

Q. And while that information is being transmitted over the serial line, is it still a PCI bus transaction? 01:40:42 01:40:44 01:40:48

MR. DAVIS: Objection to form. 01:40:54

THE WITNESS: Here I would stick to the specification and one of the functionalities and features of a specification requires that compliant devices can communicate with each other directly. So with a serialized version of this, although the entire information may be there but in a different form, one could not connect directly a PCI compliant device for it to work, it would have to be reconverted into the ordinary or defined PCI format for this to work. 01:40:59 01:41:03 01:41:07 01:41:09 01:41:13 01:41:19 01:41:21 01:41:24 01:41:28 01:41:31

BY MR. BUROKER: 01:41:35

Q. So the claims, in your reading, contemplate some sort of transformation of the PCI bus transaction into a format that is serially transmitted and then, on the other end, it would be converted back into PCI bus transaction format? 01:41:35 01:41:38 01:41:43 01:41:48 01:41:53 01:41:58

MR. DAVIS: Objection; form. 01:41:58
THE WITNESS: The patent text outlines 01:42:01
this in great detail, and this is the context in 01:42:04
which I would read this claim. Because it has to 01:42:06
be seen in the context of the patent. So yes. 01:42:12
BY MR. BUROKER: 01:42:17
Q. If you add information to the PCI 01:42:44
bus transaction is that resulting set of data 01:42:46
still a PCI bus transaction? 01:42:54
MR. DAVIS: Objection; form. 01:42:58
THE WITNESS: Can you be more specific? 01:43:01
BY MR. BUROKER: 01:43:03
Q. Right, so if there's 47 lines in 01:43:03
a PCI bus transaction, if you add five additional 01:43:06
lines of information for whatever reason, is the 01:43:12
resulting 55-bit piece of information still a PCI 01:43:15
bus transaction? 01:43:21
MR. DAVIS: Objection; form. 01:43:23
THE WITNESS: The game about standards 01:43:28
is quite clear: what is in the standard is what 01:43:29
it is, no more no less. So answering your 01:43:33
question, I say what you have now is some 01:43:37
superset of a PCI transaction, which would be 01:43:42
part of something else. That additional 01:43:44
information has no meaning with respect to the 01:43:47

PCI transaction. 01:43:49
BY MR. BUROKER: 01:43:53
Q. Right, so let me just refer you to paragraph 80 of your declaration. You discuss some of the figures from the '814 Patent, right? And 80 is fairly long with lots of figures, so if you need to read it that's fine. 01:43:53 01:43:57 01:44:09 01:44:15 01:44:18
In there you note that the inventor in these figures contemplates adding something he called bus status bits; is that correct? 01:44:20 01:44:23 01:44:26
A. Yeah. 01:44:30
Q. Okay. And then the PCI bus transaction plus these bus status bits are encoded into a form that are then set serially over a serial bus. Is that your understanding of what's shown in Figures 13, 14 and 17? 01:44:32 01:44:37 01:44:43 01:44:48 01:44:51
A. Let me just see. 14 I can see. Are you talking about the figures in the claim 13, 14, 17? I'm sorry. 01:44:58 01:45:11 01:45:15
Q. No, the figures in the patent. 01:45:16
A. 17 and 14, but where is 13? There's one. Do I have the wrong one? You're talking '814, right? 01:45:20 01:45:32 01:45:34
Q. Right, paragraph 80. Within paragraph 80, you have included -- 01:45:36 01:45:40

A. This diagram, yes, 17. 01:45:43
Q. -- Figures 17, 13 and 14 out of the '814 Patent. 01:45:45 01:45:51
A. Oh, sorry, I see this. I took the whole thing for Figure 14 and I overlooked that there is a Figure 13 on top of it. Yes, this is correct. 01:45:51 01:45:53 01:45:56 01:45:58
Q. Okay, so you're looking at the right thing? 01:45:58 01:46:00
A. Yes. 01:46:00
Q. And then you point to in your text, you say that what is the label with the red box -- let's see what number it is -- 5 are what you call bus status bits. Do you see that? 01:46:00 01:46:03 01:46:06 01:46:19
A. Yeah. 01:46:23
Q. And that's not part of a typical PCI bus transaction, these bus status bits, right? 01:46:23 01:46:26 01:46:28
A. Correct. They would have to be in the figure we just looked at on page 7 for it to be part of the standard. 01:46:29 01:46:32 01:46:36
Q. So my question to you is then is what is shown in Figure 13 and 14 a PCI bus transaction in serial form? 01:46:43 01:46:47 01:46:57
A. Now, I'm -- 01:47:04

MR. DAVIS: Objection to form. Sorry, 01:47:04
I didn't mean to interrupt. 01:47:06
THE WITNESS: If you look at page 49, 01:47:09
it says the bus status bits: 01:47:17
"... BS0 [through] BS3 in Figures 13 01:47:21
and 14 are 'bus status' bits added by the 01:47:24
inventor to facilitate serialized communication 01:47:32
and form 10 bit packets, which may include 01:47:38
PCI-related information like the FRAME ... 01:47:42
[initiator and target ready] signals." 01:47:47
So basically they put it there and have 01:47:49
given it just a different name, but this is 01:47:57
basically the placeholder for these PCI-related 01:48:01
signals. But they may have different meanings 01:48:04
depending on whether or not the signal goes 01:48:08
initiator to target or target to initiator 01:48:11
because these are unidirectional signals. 01:48:13
So the conclusion to say these are not 01:48:18
PCI signals is not exactly correct. These are 01:48:20
PCI signals, it's just a different name for 01:48:23
a kind of a placeholder, if you want to code 01:48:28
them. 01:48:30
BY MR. BUROKER: 01:48:31
Q. So they've taken the PCI-required 01:48:31
signals and created placeholders for them. Was 01:48:35

the result of that still PCI bus transaction or is it something different? 01:48:40 01:48:43

MR. DAVIS: Objection; form. 01:48:45

THE WITNESS: I mean, that discussion we had before, this is a serialized version of a PCI bus transaction which has to include everything necessary to define that transaction accurately, but this particular encoding signals on wires sequences of bits on those signals is not, in the strict sense of the specification, a PCI bus anymore, but it has everything in it to very easily recreate it, which is an important thing. One to one create it with all details in it. Right? So, for example, also the definition what is the sequence of address bits which go on to the individual signal lines because we have a tenfold increase in clock rate enabling to get the number of parallel signals appropriately down. 01:48:48 01:48:49 01:48:54 01:48:55 01:48:58 01:49:04 01:49:11 01:49:14 01:49:19 01:49:21 01:49:27 01:49:36 01:49:39 01:49:44 01:49:47 01:49:52

BY MR. BUROKER: 01:49:53

Q. So, in summary, is it your understanding that the phrase we looked at in claim 24 requires that what is communicated are all of the pieces of information needed to recreate the PCI bus transaction on the other end 01:49:53 01:49:57 01:50:00 01:50:05 01:50:08

of the serial transmission? 01:50:13
A. Right, the PC -- 01:50:15
MR. DAVIS: Just pause and let me object in between. Objection; form. 01:50:18 01:50:19
BY MR. BUROKER: 01:50:23
Q. You can answer. 01:50:23
A. I shouldn't give quick answers so that we don't have these collisions. 01:50:25 01:50:27
Q. Do you need her to read back? 01:50:27
A. Yeah, I apologize, could you? 01:50:51
(The record was read back.) 01:50:51
MR. DAVIS: Objection; form. 01:50:51
THE WITNESS: Again, and I confirm that and wish to add, of course, the PCI bus transaction initiated by the bus master at the other side of this interface. It's not any PCI bus transaction, it's the particular one on the other side of the interface. 01:50:53 01:50:56 01:50:59 01:51:02 01:51:07 01:51:10
BY MR. BUROKER: 01:51:23
Q. So, the second term that was discussed is the word "encoded" and it's paragraph 116 where that section starts and goes through 120. 01:51:25 01:51:29 01:51:34 01:51:39
So in paragraph 116 you state that you believe that the broadest reasonable 01:51:45 01:51:49

interpretation of encoded requires that it must be reversible; is that correct? 01:51:51 01:51:56

A. That's correct. 01:52:00

Q. Okay. And is that language, the reversible language, required by the IBM technical dictionary you cite? 01:52:01 01:52:08 01:52:14

A. Yes. 01:52:16

Q. Where is that? 01:52:16

A. It's a bit of a complicated language in this dictionary. Encoding -- well, I mean it defines here first of all the term "code", which is: 01:52:33 01:52:35 01:52:43 01:52:46

"A set of rules that maps the elements of one set onto the elements of another set ... The first set is the coded set and the second set is the code element set. [The] element of [one] code element may be related to more than one element of the coded set *but the reverse is not true*." 01:52:47 01:52:50 01:52:53 01:52:56 01:52:59 01:53:02 01:53:05

That means basically you have many ways of encoding but there's always the one-to-one relationship. One example the famous ASCII code, turning letters into codes. There is a one-to-one relationship for every letter being a code. For example, capital A is hexadecimal 01:53:05 01:53:07 01:53:10 01:53:15 01:53:19 01:53:22

41. And this is a one-to-one relationship. 01:53:28
Anything else wouldn't make sense because once 01:53:32
you have the code you couldn't recreate the 01:53:34
letter if there was an ambiguity. But there are 01:53:36
other codes, for example, Unicode. It turns out 01:53:39
ASCII code has limitations. It was invented in 01:53:42
America and at that time people didn't notice 01:53:47
that we have what we call umlaut in Germany, 01:53:50
accents in French, so that all doesn't exist, and 01:53:53
then the entire Arabian space where you have all 01:53:57
these different letters, so Unicode was invented. 01:54:02
While ASCII is a seven-bit code, every character 01:54:07
seven bits, Unicode is a 16-bit code, so you have 01:54:20
65,000 characters possible. And you have to now, 01:54:14
if you have a code, of course tell which is the 01:54:19
context, which coding rules that has been used, 01:54:22
but there always has to be a one-to-one 01:54:25
relationship. Or, in other words, there always 01:54:27
is a decoder for an encoder. 01:54:30

Q. Let me just hand to you the IBM 01:54:37
dictionary which was being cited here, which was 01:54:40
previously marked Acqis Exhibit 2024 in the '1469 01:54:46
IPR proceeding. 01:54:50

Do you recognize this set of pages out 01:54:51
of the IBM technical dictionary? 01:54:54

A. I recognize it. It's a bit bigger than that, yeah. 01:54:56 01:54:58

Q. Yes, a little bit bigger. 01:54:59

So you looked at the definition of "code" and there are 13 actual definitions under the word "code". You cite just one. Did you look at the others to see if they were applicable? 01:55:01 01:55:02 01:55:10 01:55:14 01:55:17

A. I mean there is a lot of different examples here, but they all fall under the same fundamental principle I state here, so I believe the correct answer here would be then yes, but we can go through them to be really absolutely sure: 01:55:27 01:55:29 01:55:31 01:55:34 01:55:37

"A set of items, such as abbreviations, representing the members of another set." 01:55:42 01:55:45

It's a generic form of encoding. 01:55:48

Q. Definition (2) doesn't explicitly say that coding requires reversibility, does it? 01:55:53 01:55:59

A. But it's in the context of the overall definition. 01:56:12 01:56:14

Q. So you read (2) in context of (1). Is that what you're saying? 01:56:18 01:56:21

A. Yeah. I mean, this is all under the section "code" anyway. And also if you use abbreviations to represent a particular member of 01:56:23 01:56:24 01:56:35

another set, how much sense does it make if this abbreviation is ambiguous? 01:56:39 01:56:44

Q. Okay. Some other terms are used in the patent but there's no explicit section, so I wanted to see if you could explain what you understood those to mean. So in claim 24 of the '814 Patent there is the phrase "northbridge" used, we've talked about that clause a number of times. What did you understand the phrase "northbridge" to mean in the context of claim 24 of the '814 Patent? 01:57:23 01:57:26 01:57:30 01:57:34 01:57:37 01:57:46 01:57:48 01:57:50 01:57:53

A. I believe I have a drawing in here which should outline that. In general as being referred to as the interface device which is interfacing the processor to the memory and some additional I/O devices which are typically then called "southbridge". And the term "northbridge" basically came from the fact that usually -- here is an example -- the processor is drawn on top and -- 01:57:57 01:58:00 01:58:05 01:58:13 01:58:17 01:58:20 01:58:22 01:58:26 01:58:29

Q. Sorry, you need to just say what you're referring to because there's no way to get that on the transcript. You're looking at what page of your declaration? 01:58:30 01:58:31 01:58:34 01:58:36

A. I'm looking at page 33 of the 01:58:38

declaration, which is Figure 1-4, called, "PCI Based System Showing Implementation of a PCI-to-PCI Bridge." 01:58:40 01:58:47 01:58:47

It's just one example of a computer. I mean here you see as an example that the northbridge functionality, in this example a chip from Intel, basically interfaces directly to the processor through its front side bus and on the other side to the main memory of that processor, here called SDRAM, to the graphics. This is an old figure, so it still has the advanced graphics port (AGP) and at the bottom has S-interface with the periphery a PCI interface where the southbridge again interfaces the PCI also and has a large number of different, much slower, typically much slower interfaces such as IDE, USB, ISA bus, and so forth. 01:58:49 01:58:53 01:58:56 01:58:59 01:59:03 01:59:08 01:59:14 01:59:17 01:59:20 01:59:24 01:59:27 01:59:30 01:59:34 01:59:40

Q. And so then the term "peripheral bridge" is used in claim 31 of the same patent. What understanding did you give to that term? 01:59:47 01:59:50 01:59:57

A. Peripheral devices a typically considered -- well, periphery to a computer to a processor could be anything like a keyboard, mouse, hard drive, network interfaces and so force. So a peripheral bridge would be 02:00:02 02:00:07 02:00:10 02:00:17 02:00:21

an interface between those devices having very 02:00:23
many different possible standards, and the 02:00:29
computer, the core of the computer. 02:00:31

Q. So claim 31 specifically says that 02:00:37
the peripheral bridge is coupled to 02:00:40
a microprocessor unit, without an intervening PCI 02:00:44
bus. So, in that particular case, the peripheral 02:00:48
bridge would have to have a connection to the 02:00:52
microprocessor and no intervening peripheral bus; 02:00:56
is that right? 02:01:00

A. This is what the claim says, yes. 02:01:01

Q. Right. And then claim 24, going 02:01:02
back, the northbridge, it states, has to be 02:01:07
directly coupled to the microprocessor unit. Do 02:01:09
you see that? 02:01:14

A. Just not yet. 02:01:16

Q. In claim 24, it says the 02:01:17
northbridge and then it says: 02:01:20

"Said north bridge directly coupled to 02:01:23
the microprocessor unit." 02:01:25

A. Yes, I see, yeah, yeah. 02:01:27

Q. And then claim 54 of the '873 02:01:29
Patent -- I'm going to have you flip to 02:01:45
a different patent -- the last element of claim 02:01:47
54 is the peripheral bridge. Do you see that? 02:01:56

A. "... directly coupled to the processing unit."

Q. Right, so in this case the peripheral bridge has to be directly coupled to the processing unit, not just coupled as in claim 31 of the '814, correct?

A. It states it that way, yes.

Q. And did you use the same understanding of the term "peripheral bridge" in your analysis of both patents? In other words claim 31 of the '814 and claim 54 of the '873 patent?

MR. DAVIS: Objection; form.

THE WITNESS: Peripheral bridge in 31 and, excuse me, 54 it was.

Yeah, in both cases, there is no further limitation on the peripheral bridge, so the definition holds.

BY MR. BUROKER:

Q. Is there any minimum set of requirements, that you can think of, that something has to have to be a peripheral bridge as understood in these claims?

MR. DAVIS: Objection; form.

THE WITNESS: I am not aware of

a definition, an official definition what has to 02:03:31
be a peripheral bridge like what is PCI standard, 02:03:37
but in this context obviously the peripheral 02:03:41
bridge has to have an interface to the processor 02:03:48
and since the limitation is made clearly directly 02:03:51
coupled in some cases, there is obviously 02:03:55
different ways to do this and obviously it has to 02:03:59
have an interface circuitry to peripheral 02:04:01
devices, one or many. 02:04:08

BY MR. BUROKER: 02:04:26

Q. So we talked about this a little 02:04:26
bit, the word in claim 24 of the '814 Patent, the 02:04:27
word "communicate" is used, it says: 02:04:32
"... the north bridge to 02:04:37
communicate ..." 02:04:38
-- and then the rest of the clause. 02:04:39
What's your understanding of what that verb 02:04:41
"communicate" means in the context of claim 24? 02:04:44
Let me strike that and say what do you 02:04:54
believe the broadest reasonable interpretation of 02:04:56
the term "communicate" is that you applied in 02:04:58
analyzing the claims versus the references in 02:05:02
these IPRs? 02:05:05

A. In this case -- and we're talking 02:05:13
now the '814 Patent, claim 24 -- the northbridge 02:05:14

which communicates, sends this information to some recipient such that it can decode the information appropriately or decode (sic). 02:05:18 02:05:22 02:05:26

Q. Do you believe communication then is limited to transmitting and does not include receiving? 02:05:28 02:05:31 02:05:35

A. I'm hesitant to answer immediately because the claim here basically doesn't specify who is receiving, but in general communication makes little sense if nobody receives the information. That is true, that is clear. It could be seen implicitly here in the claim. Obviously it's being received and used. 02:05:51 02:05:53 02:05:56 02:05:59 02:06:01 02:06:05 02:06:07

Q. But my question is whether the northbridge -- if the northbridge only received address and data bits of PCI bus transaction in serial form, didn't transmit them, would that element be met? 02:06:12 02:06:14 02:06:20 02:06:23 02:06:30

MR. DAVIS: Objection; form. 02:06:32

BY MR. BUROKER: 02:06:36

Q. You might imagine like, I know that some of these transactions we talked about are just one-way transactions. So if there was a northbridge that only received a PCI bus transaction in serial form and didn't transmit 02:06:36 02:06:39 02:06:43 02:06:46 02:06:49

anything in response, would it meet, in your 02:06:54
understanding, the requirement of this claim? 02:06:56

A. Now, two things. Yes, there are 02:06:59
communication channels but now outside of this 02:07:03
patent, which could be one-way, right? So, for 02:07:05
example, if you switch on the radio and listen to 02:07:13
the news there is a communication happening 02:07:16
between the radio broadcaster and you receiving 02:07:19
that message and there is no way of you talking 02:07:22
back. However here we have communication of 02:07:24
address and data bits of PCI bus transaction and 02:07:24
PCI bus transactions are defined here as being 02:07:33
reading and writing and that requires 02:07:34
bi-directional communication, right? Simple 02:07:39
example, a read transaction requires the bus 02:07:41
master, the initiator, to send an address to the 02:07:44
target, information goes out. But without data 02:07:46
coming back, answering that read, there is no 02:07:51
read transaction. So, the fact that this is 02:07:54
a communication of a PCI bus transaction requires 02:07:58
it to be bi-directional full duplex, as we say. 02:08:00

(The court reporter sought 02:08:00
clarification.) 02:08:00

THE WITNESS: Or a full duplex. 02:08:18

BY MR. BUROKER: 02:08:21

Q. Bi-directional, I think, right? Sir, that's what you meant to say?

A. (The witness nodded.)

Q. Yeah, I didn't want to ...

A. That might be a bit of a German accent thing.

Q. That's fine, I just want to make sure we get a clear record.

And then in claim 31, instead of the word "communicate", the language in another part of the claim says "transmit". I'm sorry, no, I meant earlier in the claim, in claim 24, if you look up there.

A. Uh-huh.

Q. There the language was that the console has an LVDS channel "that transmit encoded data".

A. Yeah.

Q. So in that situation what is your belief as to the broadest reasonable interpretation of the word "transmit" in claim 24?

MR. DAVIS: Objection; form.

THE WITNESS: I mean we have two unidirectional serial channels that transmit

encoded data of peripheral component interconnect 02:09:43
bus transactions. So every individual channel is 02:09:49
a one way thing but they are opposite direction, 02:09:53
so each of the two ones transmit their part of 02:09:57
the entire PCI transaction. It goes together. 02:10:02
BY MR. BUROKER: 02:10:02
Q. But the word "transmit" is 02:10:06
a one-way passage of data, it's just in the 02:10:11
context of the claim you're saying because there 02:10:17
are two pairs -- 02:10:19
A. Yeah. 02:10:20
Q. -- that the serial channel sends 02:10:21
things both ways; is that correct? 02:10:22
A. Yes, each and every one is 02:10:24
a unidirectional but together it is 02:10:26
bi-directional again and without that a read 02:10:30
transaction would not be possible. 02:10:34
Q. So then later on in this claim, 02:10:41
the word "convey" is used. So if you look down 02:10:45
at the phrase that starts: 02:10:49
"The second LVDS channel ..." 02:10:50
-- et cetera, et cetera, et cetera. 02:10:52
Later on in that same clause it says: 02:10:54
"... said second LVDS channel extending 02:10:57
from said north bridge to convey said address and 02:11:00

data bits of PCI bus transaction in serial form." 02:11:04
Do you see where I am? 02:11:10
A. Yeah. 02:11:13
Q. So what is the broadest reasonable interpretation of the word "convey" in the context of the claim that we just read? 02:11:14 02:11:16 02:11:17
A. This is just a different word for the same thing. The information about the PCI bus transaction is communicated or exchanged or conveyed and this is, in this case, done in serial form. I read this such that whoever constructed that claim just used a different word for it to be possibly a bit better readable. 02:11:30 02:11:32 02:11:39 02:11:48 02:11:51 02:11:57 02:12:00
Q. Okay, now looking at which patent, 54 of the '873? 02:12:11 02:12:15
A. Yes. 02:12:17
Q. Now I want to ask you about -- we may have touched on this a bit earlier -- the phrase in the second-to-last clause, there's the low-voltage differential signal, that clause. Later on it says: 02:12:32 02:12:35 02:12:38 02:12:41 02:12:44
"... to transmit data in opposite directions for communicating an ..." 02:12:47 02:12:49
-- and here's the question -- 02:12:52
"... encoded serial bit stream of ... 02:12:54

(PCI) bus transaction ..." 02:12:56
Does that mean that all of the elements 02:13:01
of the PCI bus transaction have to be encoded, 02:13:07
including the address data control signals, 02:13:13
et cetera? 02:13:18
A. Whatever pertains to the PCI 02:13:18
transaction otherwise it wouldn't be complete, 02:13:21
yeah. 02:13:23
Q. And to your understanding of the 02:13:24
broadest reasonable interpretation, the encoding 02:13:27
must be done in such a way that it's reversible 02:13:29
on the receiving end; is that correct? 02:13:32
A. Absolutely, I mean, in particular 02:13:34
also if you look at this in the context of this 02:13:38
patent it wouldn't make much sense if this 02:13:43
encoding would not be reversible because then the 02:13:47
far end would not be able to recreate the 02:13:49
transaction. 02:13:51
Q. I'll direct you to page 91 (sic) 02:14:09
of your '814 declaration? 02:14:11
A. Yeah. 02:14:31
Q. You're talking about the TNet 02:14:32
solution -- which is TNet, T-N-e-t -- from the 02:14:41
Horst reference that we'll be talking about 02:14:41
shortly. But you say: 02:14:44

"The TNet solution, discussed in the Horst reference, was not solving the same problem as that encountered by Dr. Chu in the '814 patent." 02:14:45 02:14:48 02:14:51 02:14:54
Do you see where I'm talking about? 02:14:55
A. Not quite yet. 02:14:57
Q. The very first sentence of paragraph 91. 02:14:59 02:15:00
A. Oh, I have page 91. That's something else. 02:15:01 02:15:05
Q. Oh, that's not the same. 02:15:06
A. Yes. I'm right there. 02:15:12
Q. Okay. So is it your understanding that a prior reference has to be solving the same problem as the inventor in order to invalidate it? 02:15:13 02:15:21 02:15:25 02:15:32
A. No, it does not. 02:15:32
Q. So what was the reason that you said they're not solving the same problem? 02:15:33 02:15:35
A. Whatever has been cited as prior art has to make sense as a functioning system if put together and, I mean, this is just the introductory sentence to a rather long chain of arguments, where these things are detailed more. So taking out of context, yes, this is not enough 02:15:41 02:15:45 02:15:49 02:15:53 02:15:57 02:16:03

to make this plain. The fundamental difference between these two scenarios, what is described in the patent and what is outlined in the Horst reference is basically one is a parallel computer system, supporting up to, I believe, a million of nodes, where the other is something where you have one single computer with a completely confined context and functionality allowing to connect an I/O subsystem or a console in a highly efficient way. So many of the things required in this context to be there would hinder what is disclosed by Chu and if one would try to introduce, to basically impose what is disclosed by Chu on TNet it wouldn't work anymore, you have a single address base in PCI and you cannot possibly have that in such a distributed system. 02:16:05 02:16:12 02:16:17 02:16:20 02:16:24 02:16:26 02:16:30 02:16:33 02:16:38 02:16:43 02:16:51 02:16:57 02:17:00 02:17:04 02:17:07 02:17:10

Q. So it's not your understanding, and you were not trying to, as part of your invalidity analysis, determine that the claims solved the same problem as the prior art? That was not something that you felt like you had to find in order for there to be invalidity, right? 02:17:16 02:17:18 02:17:23 02:17:27 02:17:29 02:17:31

Let me ask that again. 02:17:35

You were not operating under the understanding that to show something is invalid, 02:17:38 02:17:39

a claim is invalid based on a reference that the 02:17:41
claim and the reference are addressed to the same 02:17:44
problem? 02:17:47
A. This is not a requirement, but if 02:17:50
you ask about the basics of the analysis, I have 02:17:51
that outlined, starting at page 10, right? I 02:17:58
mean this is the whole claim construction 02:18:02
business. In particular this is about 02:18:05
anticipation and obviousness, right? And both 02:18:08
principles I have applied to the best of my 02:18:13
knowledge. I guess the most important one is 02:18:15
about obviousness, right? Most of the claims 02:18:19
which are under discussion here are on the 02:18:25
obviousness issue. I mean there's quite a bit of 02:18:29
text which I put in, you know, hoping to make it 02:18:35
clear. 02:18:39
Q. So you just mentioned that one of 02:18:40
the differences with Chu and the Horst reference 02:18:43
had to do with addressing and you indicate that 02:18:47
the Horst reference uses virtual addressing; is 02:18:54
that correct? 02:18:57
A. This is correct and it is stated 02:18:58
in the Horst reference which means now would be 02:19:00
a good time -- 02:19:03
Q. Do you need a copy? 02:19:05

A. -- to have it so that I can point you to, if I can find it quickly. But it makes a clear point, and there is also a technical requirement for this to be the case. It's similar in SCI. 02:19:06 02:19:08 02:19:12 02:19:15 02:19:22

Q. So this is Horst, which is 1009 in '814 IPR but it is also 1011 in the '873 IPR. So I'm giving you the copy that was marked 1009 in the '814. 02:19:25 02:19:31 02:19:38 02:19:41

So my question I was going to ask you is really about virtual addressing versus physical addressing which you say that PCI devices use physical addressing; is that correct? 02:19:54 02:19:59 02:20:03 02:20:08

A. Yes. 02:20:10

Q. And is it your understanding that the claims that are at issue in these IPR proceedings exclude virtual addressing? 02:20:12 02:20:14 02:20:18

MR. DAVIS: Objection; form. 02:20:22

THE WITNESS: I mean you now ask for all claims? 02:20:26 02:20:27

BY MR. BUROKER: 02:20:29

Q. No, no, the claims in the IPR proceedings, we can start with claim 24 in the '814. Is there any language you were looking at where it says virtual addressing is excluded? 02:20:29 02:20:31 02:20:34 02:20:38

A. It says always in the context of addresses, addresses of PCI bus transaction. Since PCI bus transactions are meant, it has to be physical addresses. So this is basically part of the context of it being PCI, right?

And let me maybe to have a clean differentiation between a virtual and physical addresses, because I'm sure we will have more of that. The important thing is a physical address enables to locate the particular device or the particular word in memory unambiguously. This is what it is. Unlike a virtual address. And since these claims are about the physical I/O bus PCI using physical addresses, because in here the PCI address is used to select the device connected on the bus, and there could be any number of devices connected there. It has to be a physical address. The final result of any physical-to-virtual -- sorry, virtual-to-physical address translation. I misspoke.

Q. Would you agree the claim 24 contemplates the creation of a serial form of the PCI bus transaction?

A. I mean I would stick to the exact claim language and, I mean, it says really

clearly: 02:22:53
"... serial channels that transmit 02:22:55
encoded data of Peripheral Competent Interconnect 02:22:57
(PCI) bus transaction in opposite directions ..." 02:23:03
-- saying the PCI transaction is 02:23:04
communicated in serial form. That doesn't 02:23:08
constitute that a new standard is created calling 02:23:11
it a serial PCI bus, and I don't think there is 02:23:15
any attempt in here. This is something which was 02:23:19
invented in order to avoid all the complications 02:23:23
with big high pin count connectors limiting the 02:23:27
speed of communication for a very specific 02:23:31
purpose. 02:23:34

Q. As part of communicating the PCI 02:23:38
bus transaction in serial form, couldn't you 02:23:46
create or use virtual addressing as part of that 02:23:50
serial communication? 02:24:00

MR. DAVIS: Objection; form. 02:24:04

THE WITNESS: We have a bus here, which 02:24:07
is identified to address physical devices. 02:24:14
Communicating a virtual address on such a bus 02:24:21
would not allow the direct addressing of such 02:24:25
devices, therefore it wouldn't make any sense. 02:24:29
Basically all computers when communicating with 02:24:33
I/O devices have done their address translation 02:24:41

beforehand. 02:24:45

BY MR. BUROKER: 02:24:47

Q. So by that explanation, for this claim to make sense, then no matter what device receives this information, it has to be using a PCI bus address that is understood and known by the northbridge that sent it; is that right? 02:24:47 02:24:52 02:24:56 02:25:03 02:25:09

MR. DAVIS: Objection; form. 02:25:16

BY MR. BUROKER: 02:25:21

Q. Let me strike that and let me start over. 02:25:21 02:25:22

So if I'm going to take a PCI bus transaction and I'm going to serialize it, and on the other side it's going to come back and be recreated, any PCI device on the other end of that serial transmission has to be using the same addressing scheme as the transmitting side, correct? 02:25:23 02:25:25 02:25:29 02:25:32 02:25:34 02:25:37 02:25:42

A. It's part of the overall address map of the computer, correct. But -- 02:25:43 02:25:46

Q. So you couldn't have, in that situation, a PCI device on one side of the serial transmission and then one on the other one that has the same address? 02:25:50 02:25:53 02:25:58 02:26:00

A. No. 02:26:02

Q. It wouldn't work?

A. Not a good thing.

Q. You would have a collision, correct?

A. Correct. This is actually one of the fundamental differences in the big new thing which came about in the context of PCI because that is one of the big issues we had with VME, which is also part of the prior art being cited here so it makes sense. In VME the address map had to be defined before you switch on the computer and you do this on a piece of paper and then you had a little row of switches on all the I/O devices where you defined this is your slave address, and if by accident you enable two devices on the same slave address you have a non-working computer which even could end up in hardware damage.

In PCI the system works differently. When your computer wakes up all devices are basically dead, disabled, do nothing. Then the computer basically goes step by step through the entire PCI tree, and this can be quite a few devices, potential devices. It will address every particular physical slot in the computer

connection device and this is why PCI has to have geographic addressing which is part of the configuration cycles. This is why I said configuration is a little bit different in each one. So the computer goes through every slot, every potential location for an I/O device and once it finds such a device, then it will check what is the amount of local memory I/O space the device has, collect all that information, then the BIOS creates an address map, based on some algorithm which is not disclosed, and then it goes back and writes to every individual PCI device, "This is now your base address on which you respond if there is ever a PCI transaction." And, of course, it's being made very sure that under no circumstances windows overlap because then you have two devices answering and the result is garbage. That means, and this is why I said earlier, without PCI configuration cycles you have nothing, you have a dead system. And that also means, taking into account now the Horst reference, you have a million possible nodes and each of those million nodes could have several tens of possible PCI devices depending on the complexity of the PCI tree, this what is 02:27:11 02:27:16 02:27:17 02:27:20 02:27:23 02:27:26 02:27:30 02:27:34 02:27:38 02:27:41 02:27:46 02:27:48 02:27:50 02:27:53 02:27:56 02:27:59 02:28:03 02:28:06 02:28:10 02:28:12 02:28:14 02:28:17 02:28:20 02:28:25 02:28:28

called device war would have to be done across all these devices and it could only be done by one because the address map is something which is seen centric to one processor. So the entire PCI architecture basically assumes there is one processor at the top which defines the address map. And even today in multiprocessor computers it's exactly like that. 02:28:31 02:28:34 02:28:37 02:28:42 02:28:45 02:28:48 02:28:50 02:28:54

Q.   The patent, both patents, give examples of different ways of transmitting PCI bus transaction in a serial form, we were looking at 13, 14 and 15, Figures 13, 14, 15, right? 02:29:12 02:29:15 02:29:21 02:29:26

MR. DAVIS: Objection to form. 02:29:32

BY MR. BUROKER: 02:29:32

Q.   For example. 02:29:32

A.   Which patent? 02:29:34

Q.   '814. 02:29:36

A.   Okay, let me just pull this out. 02:29:38

Q.   13, 14 and 17, sorry. 02:29:43

A.   You mean 13A and B? 02:29:51

Q.   Actually, you know what, I think it's the '873 Patent. 02:29:53 02:29:54

So, yeah, your paragraph 80 earlier, we were looking at Figures 13 and 14 of the '873 Patent. 02:30:08 02:30:12 02:30:17

A. Yes. 02:30:17
Q. And then Figure 17 of the '814 02:30:17
Patent. 02:30:22
A. Yeah, these are just the 02:30:22
differential signals, right, the 17. Yeah. 02:30:29
Q. Well, 17 is showing what would be 02:30:33
used to generate the signals on the serial line, 02:30:38
right? 02:30:42
A. The clock and the four signals 02:30:43
conveying the actual ... 02:30:46
Q. Right, that would be a five-wire 02:30:49
system, and since there are five wires and 02:30:50
there's way more bits than that, that makes it 02:30:52
a serial transmission in your view; is that 02:30:56
correct? 02:30:58
A. Yeah, according to the definition 02:30:58
I set forth. 02:31:03
Q. Okay. And doesn't the 02:31:04
specification also say that the XP bus, which is 02:31:05
the serial bus in the patent, can use IEEE 1394? 02:31:11
MR. DAVIS: Objection; form. 02:31:20
THE WITNESS: Now, where does it say? 02:31:25
Where are we referring to and which patent? 02:31:27
BY MR. BUROKER: 02:31:31
Q. So '814, column 22, lines 7 to 8. 02:31:31

A. Column 2 you're saying? 02:32:05

Q. Column 22. 02:32:07

A. Sorry. 02:32:08

Q. Yes. 02:32:37

A. Yeah, I see that. I mean basically what it says here is what we have here is one way of communicating signals in a very efficient and fast way, and this is not limited to PCI itself, yeah. 02:32:37 02:32:40 02:32:43 02:32:46 02:32:49

Q. Right. So starting at column 22, line 4, it says that: 02:32:59 02:33:01

"The XP Bus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment the XP Bus lines may be IEEE 1394 lines." 02:33:02 02:33:15 02:33:20 02:33:26 02:33:29 02:33:32 02:33:38

Right? That's saying that the bits that are used to transmit the serial form of the PCI bus can be IEEE 1394, FireWire line? 02:33:38 02:33:42 02:33:47

MR. DAVIS: Objection; form. 02:33:55

THE WITNESS: Do you have the 1394 standard right handy? 02:33:58 02:34:15

BY MR. BUROKER: 02:34:19

Q. I don't know that I do. You're familiar with it obviously.

A. Sure.

Q. And what is it generally?

MR. DAVIS: Objection to form.

BY MR. BUROKER:

Q. I don't have a copy.

A. This evolved from the SCI standards. Dave James, one of the main authors of SCI, was also on the FireWire 1394 Committee I believe when he still was working for Apple. The reason why I wanted to have a quick look is to refresh my mind about the exact physical signalling definition in 1394.

The point here is obviously about the definition, what is LVDS. And there is, on one hand, the IEEE 1596.3 standard, which is, I believe, the first incarnation of LVDS. In fact that was just when I arrived in the U.S. as a post-doc I was even part of that working group and I saw the very first LVDS chips of national semiconductors ever to exist, and they were defined in the 1596.3 standard, a substandard of SCI. Later, slightly different versions were created, and I believe the patent says clearly

that in case of LVDS being cited they mean 02:35:58
generic low-voltage differential signals. So the 02:36:04
bottom line is, for example, 1596.3 says the 02:36:07
midpoint of that signal has to be at 1.2 volt and 02:36:12
the signal is, I believe, a one milliampere 02:36:15
signal, so if you want to move it to 1.5 volts it 02:36:19
wouldn't be LVDS any more according to 1596.3 02:36:22
but, from the context, from the logical meaning 02:36:26
-- what is low-voltage differential very 02:36:29
high-speed signals -- it would still be the same 02:36:36
thing. 02:36:38

So what they try to say here is, in my 02:36:38
understanding, if a slight variation of the 02:36:43
physical signalling from the original standard, 02:36:45
it would still work the same way, it would still 02:36:51
make sense. 02:36:56

I'm trying to find now the definition in 02:36:57
this patent, how they interpret LVDS, but I'm 02:36:59
very sure there is a definition and it says that. 02:37:02

Q. Well, in paragraph 81 of your '814 02:37:08
declaration, it says: 02:37:13

"The '873 patent discusses serial lines 02:37:21
and serial packet protocols and uses LVDS IEEE 02:37:24
1394 (FireWire) and Universal Serial Bus ... as 02:37:29
examples." 02:37:33

And then you cite to the '814 Patent column 22, 26 to 30. I don't know if that's helpful. 02:37:34 02:37:37 02:37:44

And then it says: 02:37:45

"... LVDS encodes serial bits as voltage differences onto opposed lines such as in Figure 15 of the '873 patent." 02:37:48 02:37:51 02:37:54

A. You got me lost, I wasn't fast enough for you. Which page are we now? 02:37:56 02:37:59

Q. Paragraph 81, page 49. 02:38:01

A. '814, 22, 26 to 30. Yeah, I mean here they also say they are examples but they don't limit themselves to any particular special incarnation. 02:38:59 02:39:12 02:39:15 02:39:20

Q. Does IEEE 1394 support 32-bit PCI flat addressing? 02:39:22 02:39:30

A. Now, I would really like to look at that specification. Off the top of my head this is a different thing and I would expect not, but I would rather look at the specification. 02:39:34 02:39:35 02:39:37 02:39:42

Q. I don't have it, I apologize. 02:39:46

A. Do we have it? 02:39:47

Q. I don't. And that's fair. As you sit here today, you don't know whether or not IEEE 1394 supports the 32-bit PCI flat addressing 02:39:48 02:39:59 02:40:01

space or not. It may or may not, is that fair? 02:40:07
A. Yeah. 02:40:09
Q. Okay. Do you know whether IEEE 1394 can contain PCI standard addresses or standard bus commands? 02:40:11 02:40:21 02:40:26
MR. DAVIS: Objection; form. 02:40:28
THE WITNESS: And I would again like to refer to the specification. If I had a computer I could pull it from the net real quick. 02:40:32 02:40:33 02:40:36
This is an SCI-like network, so consequently, given the arguments I set forth here, most likely they are the same. 02:40:40 02:40:48 02:40:52
BY MR. BUROKER: 02:40:57
Q. So you say "set forth here", your hand is on your declaration, meaning the arguments you made about SCI in your declaration about why it doesn't meet the claims you would think that IEEE 1394 doesn't meet the claims? 02:40:57 02:40:59 02:41:01 02:41:03 02:41:07
A. Yeah, but I mean I'm under oath here, I really don't want to do too much speculation and although I am obviously quite familiar with FireWire, I would rather stick to the documents and if we can't have them it's going to be a bit too much vague, I think. 02:41:11 02:41:16 02:41:18 02:41:26 02:41:30 02:41:31
MR. BUROKER: Okay. I may come back to 02:41:36

it, I can always print at some later time or for tomorrow, so we'll see.

I need to take a break right now though. Can we go off the record?

(Brief recess taken 2:41 p.m. - 2:51 p.m.)

BY MR. BUROKER:

Q. So, paragraph 82 of your declaration -- it may be even on the same page, great -- you talk about one of the advantages of the patented system is that, in the second sentence you say:

"... no new drivers are needed to ensure the peripherals work on the system."

Do you see that?

A. Absolutely, yes.

Q. Okay. So, as you read the '814, and '873 Patents, did the inventor create any additional drivers or not?

A. I believe they even make the point this is not necessary and this is a big advantage because otherwise the ACM couldn't use any generic device being connected to the console where it's plugged in. Now let me see if I can find this quickly. Probably you know this even better than me, but it's definitely in -- I

believe it's in both of them. 02:53:08

Q. Well you cite in your declaration to the '873 Patent at column 4, lines 50 to 58. 02:53:10 02:53:12

A. So I should just read my own declaration and use the references right there. 02:53:20 02:53:22

Yeah, I think the relevant sentence would be: 02:54:18 02:54:20

"The invention also can be implemented without changes in operating system and application software." 02:54:21 02:54:23 02:54:26

Now, that clearly means device drivers because they're part of the operating system and being loaded on demand depending on in fact PCI configuration cycle. 02:54:28 02:54:31 02:54:34 02:54:40

Q. Looking now at the claims we've been looking at, take for example claim 24 of the '814, is there anything in the claim that says you can't have new drivers or that, you know, the system has to be interoperable with existing software? 02:54:44 02:54:48 02:54:52 02:54:58 02:55:02 02:55:06

MR. DAVIS: Objection; form. 02:55:11

THE WITNESS: I just read it again to be really sure. It doesn't say explicitly, but since we have the transmission of encoded PCI bus transactions, that means the PCI infrastructure 02:55:13 02:55:45 02:55:52 02:55:59

is maintained and that would have a direct 02:56:06
consequence. But it's not an explicitly stated 02:56:10
requirement of claim 24. 02:56:18
BY MR. BUROKER: 02:56:18
Q. Okay. And then your declaration 02:56:20
also makes mention about the fact that there is 02:56:22
no need for any new hardware; is that correct? 02:56:27
A. In what context? 02:56:37
Q. Well, in paragraph 97 and 98, one 02:56:43
of the points you make about the difference 02:56:58
between the patented invention and the TNet 02:57:01
system is that the TNet required new hardware to 02:57:04
operate; is that correct? 02:57:07
A. Yeah, correct. 02:57:09
Q. Is there anything in claim 24 of 02:57:10
the '814 Patent that excludes the addition of new 02:57:13
hardware? 02:57:18
A. There is no statement about that 02:57:27
in this claim. 02:57:30
Q. And what about 31 of the '814 02:57:32
Patent? 02:57:34
A. Same here, no explicit language, 02:57:58
although since we are conveying complete PCI bus 02:57:59
transactions it would be implicitly the case. 02:58:05
Why build it? There's no need to build 02:58:08

additional hardware to generate the PCI transactions, because it's already here, this is the point I'm trying to make, all right? In this case PCI bus transactions are communicated over these kind of channels, it is spelt out in slightly different forms, but it's always the same basic principle, enabling the receiving device to produce that particular piece of transaction completely transparently to hardware and software. Therefore there is no need to do anything else. In case --

Q. Well if the -- I'm sorry.

A. In case of both SCI and TNet, there is an entirely radically different topology in architecture and for it to interface to PCI one has to have a particular device creating such PCI transactions based on some macro commands being sent over that network.

Q. But even the invention contemplates some additional hardware; there's the hardware that serializes the PCI bus transaction. That's a new piece of hardware, right?

A. That is correct.

Q. So what did you mean by saying

that unlike the invention TNet requires new hardware? 02:59:25 02:59:30

MR. DAVIS: Objection; form. 02:59:32

THE WITNESS: Now, let me just check, are we discussing here in context of TNet or in context of SCI? I think this is TNet, right? 02:59:38 02:59:46 02:59:50

BY MR. BUROKER: 02:59:56

Q. Correct. 02:59:56

A. Right, so these interfaces here have to have quite a bit of functionality, there is no direct obvious one-to-one A-B-C-D kind of path as to how they are to be built. They have to be able to execute all the specified PCI transactions on the remote PCI bus, but these transactions do not exist inside the TNet system area network. There is on top of that an address translation which needs to be done in the peer system, let alone it being initialized and everything. For it to be performing there is typically a very large complexity of additional functionality needed for this to make any sense. So this is a highly complex ASIC. 02:59:57 03:00:02 03:00:06 03:00:13 03:00:16 03:00:21 03:00:24 03:00:28 03:00:31 03:00:35 03:00:39 03:00:43 03:00:47 03:00:51

What is outlined in this patent is complex also, but we are basically serializing the particular ongoing PCI transaction which is 03:00:57 03:00:59 03:01:03

being then made parallel on the far end again. This is a different thing, there is no address translation for instance involved and all the other things. We can go into details here, if you want, to make this more clear. 03:01:05 03:01:09 03:01:11 03:01:12 03:01:15

Q. But my -- strike that. 03:01:23

My question was more, on paragraph 97, for example, it talks about avoiding the requirement imposed by TNet of designing new bus interface devices and new device drivers, but do you agree that to implement the '814 patent you still have to create a new hardware system to serialize the PCI bus transaction on one end and then interpret it on the other to output the PCI bus transaction on the receiving end, right? 03:01:25 03:01:27 03:01:34 03:01:40 03:01:43 03:01:50 03:01:53 03:01:56 03:02:01

MR. DAVIS: Objection; form. 03:02:03

THE WITNESS: The '814 Patent outlines how to build the serializer, this is correct. 03:02:06 03:02:14

BY MR. BUROKER: 03:02:14

Q. So there is some new piece of hardware, software, whatever it is, the serializer is something new? 03:02:17 03:02:18 03:02:20

A. Not software, hardware. 03:02:21

Q. So in the '814 Patent the patent talks about the host interface controller and 03:02:51 03:02:57

then the peripheral interface controller, the HIC and the PIC, are you familiar with those? 03:03:00 03:03:04

A. Uh-huh, let me just pull it. Okay, here we are. 03:03:08 03:03:10

Q. So those are not off-the-shelf components, correct? 03:03:15 03:03:18

A. Now, let me just see where exactly are we talking to? 03:03:21 03:03:24

Q. Well they talk about them quite a bit in the patent, so the HIC and the PIC. 03:03:27 03:03:28

A. Just to start at some particular reference to be on the same page. 03:03:35 03:03:42

Q. Which patent are you looking at? 03:03:44

A. '814. Didn't you say '814? 03:03:46

Q. That's fine. So they're shown in Figure 7 is one place. And they're in 21 and 22, they're in a number of places. 03:03:49 03:03:52 03:04:16

A. My '814 patent doesn't have a Figure 7. 3, 4, 5, 5A, 6, 8. 03:04:18 03:04:20

Q. Oh you know what, I was looking at the '873, I apologize. Let me look at the '814. 03:04:26 03:04:28

So if you look at Figure 15, for example, the top section is the host interface controller and the bottom section is the peripheral interface controller. 03:04:55 03:04:58 03:05:00 03:05:03

A. Okay.
Q. So the question is: those are not described as being off-the-shelf components in this patent, are they? 03:05:13 03:05:15 03:05:18
A. No. In particular, I mean, the XP bus is part of the patent, so this is something novel. 03:05:22 03:05:25 03:05:28
Now, I can't tell whether or not Acqis decided to make those commercial products and sell them off the shelf, so from that point of view I can't answer the question. But it's certainly not a generic something. 03:05:30 03:05:34 03:05:36 03:05:38 03:05:41
Q. Right. So, in other words to make at least the embodiments disclosed in this figure work they had to create a host interface controller, the XP bus and a peripheral interface controller, so three pieces of hardware, right? 03:05:43 03:05:45 03:05:50 03:05:54 03:05:58
A. There is quite a bit of similarity between these tools, so it's probably two versions of one common reference, right? I mean the bus controller, which is a bi-directional bus, will be mostly the same except for the clock generation, which is detailed in here, the PCI interface is the same anyway. So from that point of view they are rather similar but, yes, they 03:06:02 03:06:04 03:06:06 03:06:08 03:06:12 03:06:15 03:06:21 03:06:23

are different devices which are needed for this communication to happen. 03:06:26 03:06:28

Q. So like TNet, where you had to create additional hardware, this invention also contemplates creating additional hardware in order to send the PCI bus transaction in serial form, right? 03:06:34 03:06:37 03:06:40 03:06:43 03:06:47

A. This invention transmits PCI transactions in serial form, TNet does not. 03:06:52 03:06:57

Q. Right, but this invention, in order to do so, had to create new hardware to make that possible? 03:06:59 03:07:01 03:07:03

A. I agree with that. 03:07:05

Q. Right, you've got the Horst/TNet reference in front of you? 03:07:13 03:07:17

A. Horst/TNet, here we are. 03:07:27

Q. So one of the things you say in your declaration, and in particular -- and I'll give you the paragraph number -- is that the TNet bus interface in the console generates a PCI bus transaction; is that correct. 03:07:55 03:07:57 03:07:59 03:08:03 03:08:11

A. Where is that? 03:08:13

Q. Paragraph 133. 03:08:15

A. And we are still -- 03:08:16

Q. Oh '814 declaration, 03:08:17

paragraph 133. 03:08:20
A. Right: 03:08:37
"The TNet bus interface then uses its 03:08:37
knowledge of the PCI bus and the PCI bus protocol 03:08:40
... to generate a PCI bus transaction on the PCI 03:08:44
bus." 03:08:47
Q. Maybe it's easier if we just walk 03:08:49
through your understanding of how something would 03:08:52
work. 03:08:57
So looking at Figure 2 of the Horst 03:09:01
reference. Okay, so what is shown there is CPU 03:09:07
memory boxes up top. Those are what EMC contends 03:09:14
to be the modules, correct? 03:09:24
MR. DAVIS: Objection; form. 03:09:27
BY MR. BUROKER: 03:09:30
Q. In the claim there is an ACM 03:09:30
module, an ACM? 03:09:33
A. Yeah, I very well remember that. 03:09:36
We're talking the '814 here, right? 03:09:38
Q. Uh-huh. 03:09:42
A. So let me just pull this up 03:09:43
because I believe the definition of the ACM is in 03:09:46
the claim and it required a bit more than just 03:09:48
CPU and memory. And, I mean, this is a very, 03:09:50
very high-level diagram, so one has to be always 03:09:56

careful with these high abstraction levels. One 03:09:59
can interpret a lot into them which may not 03:10:02
really be there at the end. 03:10:06
So let me just check. 03:10:07
"... the console comprising a first low 03:10:15
voltage differential signal channel ... 03:10:18
comprising two unidirectional serial channels 03:10:20
that transmit encoded data of ... (PCI) bus 03:10:22
transaction in opposite directions; said ACM 03:10:25
comprising a microprocessor unit ... a mass 03:10:29
memory storage device ..." 03:10:31
Which is not here on top of Figure 2: 03:10:32
"... a north bridge to communicate 03:10:38
address and data bits of PCI ..." 03:10:39
Neither a northbridge is shown here nor 03:10:41
PCI is shown here. In fact it is shown that 03:10:45
these two links go to two apparently different, 03:10:47
possibly redundant, TNet sub-nets and that 03:10:54
clearly rules out PCI to be there. 03:10:59
"... a main memory coupled to said 03:11:02
processor unit through said north bridge ..." 03:11:04
Now here's the limitation that the main 03:11:07
memory has to be coupled to the CPU through the 03:11:08
northbridge, there's no northbridge shown but, 03:11:11
again, at this abstraction layer it could have 03:11:12

been just omitted. It wouldn't be something extremely uncommon to use a northbridge. A second LVDS channel, again to communicate PCI bus transaction. So, taking claim 24 as the first big independent claim of that patent, I would say this cannot be an ACM. 03:11:15 03:11:19 03:11:23 03:11:29 03:11:34 03:11:36

Q. Looking at Figure 7 then, which is a little bit of a more blown up or detailed view of the various components. 03:11:38 03:11:43 03:11:47

A. Okay. 03:11:49

Q. Let's just suppose that that RISC CPU wants to talk to a PCI device that's connected to the TNet links and the PCI device would be something hanging off the bottom of what's shown in Figure 8. 03:11:54 03:11:58 03:12:13 03:12:17 03:12:19

MR. DAVIS: Objection; form. 03:12:24

THE WITNESS: Now careful; Figure 8 is VME. 03:12:34 03:12:37

BY MR. BUROKER: 03:12:40

Q. No, Figure 8 says it can be connected to a 32-bit bus which can be VME, Motorola 68040 or PC -- it says PCL but it's referring to PCI. 03:12:41 03:12:43 03:12:51 03:12:54

MR. DAVIS: Objection to form. 03:12:55

THE WITNESS: You mean this is a typo? 03:12:56

BY MR. BUROKER: 03:12:58
Q. Yes. 03:12:58
A. A typo? 03:12:58
Q. You can go to the text, if you 03:12:59
like, just to the left of that. The text says: 03:13:00
"Figure 8 shows a block diagram of the 03:13:03
TNet bus interface (TBI) ASIC. The TBI 03:13:05
translates transfers on the standard bus into 03:13:12
TNet read or write transactions that travel 03:13:14
through TNet links to main memory. 03:13:17
"Different versions of the bus 03:13:18
interface logic support industry standard buses 03:13:20
such as VME and the peripheral component 03:13:24
interconnect (PCI), or microprocessor buses such 03:13:27
as that of the Motorola 68040 chip." 03:13:32
Do you see that? 03:13:36
A. Okay. 03:13:38
Q. So that "PCL" is a typo. It 03:13:38
should be "PCI". 03:13:40
MR. DAVIS: Objection; form. 03:13:40
BY MR. BUROKER: 03:13:40
Q. Do you agree? 03:13:41
MR. DAVIS: Objection; form. 03:13:42
THE WITNESS: Given that the text 03:13:49
clearly describes that, then I would take this as 03:13:52

a high-level diagram which says there are different versions of this obviously, which probably have different bus interfaces sitting next to each other on that ASIC in order to generate the particular type of bus transaction required. 03:13:57 03:14:01 03:14:03 03:14:07 03:14:13 03:14:16

BY MR. BUROKER: 03:14:17

Q. Right. And looking back at Figure 2, it shows an example of one of those interfaces you're talking about, it shows a box that says "PCI interface", do you see that? 03:14:17 03:14:19 03:14:24 03:14:27

A. Yes, at the right bottom. 03:14:30

Q. So looking at the Figure 8 in combination with Figure 2, what you're saying is there would be a PCI interface box that would be attached to the long line in Figure 8. Is that correct? 03:14:35 03:14:38 03:14:40 03:14:42 03:14:48

MR. DAVIS: Objection; form. 03:14:49

THE WITNESS: There would be a PCI interface connected to this bus line, the long line as you call it, drawn in Figure 8, yeah. Assuming that "PCL" is a typo, correct. 03:14:57 03:14:59 03:15:03 03:15:07

BY MR. BUROKER: 03:15:15

Q. And then connected to that PCI bus interface would be potentially one or more PCI 03:15:15 03:15:19

devices? 03:15:22

A. Correct. 03:15:22

Q. So both Figure 7 and Figure 8 refer to or point to this thing that says TNet links? 03:15:30 03:15:34 03:15:38

A. Correct. 03:15:39

Q. So the idea is that what's shown in Figure 7 would connect to the TNet links to what is shown at Figure 8. Is that the right way to read this? 03:15:40 03:15:42 03:15:46 03:15:49

MR. DAVIS: Objection; form. 03:15:50

THE WITNESS: I mean TNet is a defined protocol here and now I purposefully avoid the word "standard" because, you know, it's proprietary I assume. But it's defined, at least within the context of this document, and so TNet link in Figure 8 would have to be the same thing as TNet link in Figure 7 and they would have to be interoperable for this to make any sense. 03:15:52 03:15:56 03:16:00 03:16:04 03:16:08 03:16:12 03:16:16 03:16:20

BY MR. BUROKER: 03:16:20

Q. And then what's shown in Figure 2, those long rectangles, are described as TNet links in the document. 03:16:23 03:16:26 03:16:29

THE WITNESS: Careful, this is -- 03:16:31

MR. BUROKER: Is that right? 03:16:33

MR. DAVIS: Objection; form. 03:16:34
THE WITNESS: -- this is the TNet 03:16:36
system area network, where the TNet links are 03:16:39
only a small fraction of. The link is basically 03:16:42
just the way to connect to the system, and I mean 03:16:46
the network system here. 03:16:52
Again, also here, we are talking very 03:16:56
fast links which are point-to-point. So in order 03:16:59
to be able to have a large number of particular 03:17:03
devices talking to each other, typically with 03:17:06
lots of processors, there has to be some kind of 03:17:08
a network, with switches, routers and everything. 03:17:11
Figure 9 gives a rough outline of this. And the 03:17:15
fact that Figure 2 shows two different networks 03:17:18
here, X and Y, indicates that there is 03:17:24
a redundancy in the network, allowing packets to 03:17:33
travel different paths from source destination, 03:17:36
which is something people like to do in order to 03:17:40
have flexibility and in order to avoid 03:17:45
congestion, taking the B path if A is overloaded, 03:17:52
which has lots of highly complex ramifications. 03:17:56
So in here is a rather complex networking in 03:17:58
between. You see in Figure 9 six routers being 03:18:03
drawn. Whatever number there is depends on the 03:18:06
architecture of the switching technology being 03:18:12

developed for TNet, but there is absolutely 03:18:14
nothing disclosed, if I remember correctly, 03:18:17
inside this document as to how these switches 03:18:21
would really work in detail, except for this very 03:18:23
high-level diagram in Figure 6. Which is 03:18:29
a diagram which is basically valid for every kind 03:18:34
of switch in any kind of networking standard. 03:18:36

BY MR. BUROKER: 03:18:36

Q. Okay. So one configuration is 03:18:43
possible to have a single -- to have the elements 03:18:51
of Figure 7 connected directly over TNet links to 03:18:57
what's shown in Figure 8 and then have Figure 8 03:19:05
connected to a PCI bus interface which would be 03:19:10
connected to a PCI device? 03:19:14

MR. DAVIS: Objection -- 03:19:18

BY MR. BUROKER: 03:19:19

Q. Is that right? 03:19:19

MR. DAVIS: Objection; form. 03:19:20

THE WITNESS: Honestly I can't tell. 03:19:22
The reason is it depends really on a lot of 03:19:25
details as how this network is being built. 03:19:33
There are networks which do not allow direct 03:19:38
node-to-node connection. Basically what you're 03:19:42
saying do away without the switching and the 03:19:44
infrastructure and do a point-to-point 03:19:47

connection, I understand that. Some networks allow doing that, some don't. Whether TNet supports this functionality is not disclosed in this document. 03:19:50 03:19:53 03:19:56 03:19:58

BY MR. BUROKER: 03:19:58

Q. So the fact that there's the word "TNet link" in Figure 8 and the word "TNet link" in Figure 7, you can't tell, is what you're saying, whether or not that means that they can be directly coupled together without more information? 03:20:01 03:20:03 03:20:07 03:20:09 03:20:11 03:20:13

MR. DAVIS: Objection; form. 03:20:13

THE WITNESS: "TNet link" only means the connection for the network, very oversimplifying the network cable. But I mean it is more, right, the entire definition of the standard, protocols, and so forth. Whether or not you can directly connect them it doesn't implicitly say. So at the time this was invented, for example, it was not possible to connect two computers with a twisted pair Ethernet cable. 03:20:16 03:20:19 03:20:25 03:20:26 03:20:28 03:20:32 03:20:37 03:20:41 03:20:45 03:20:53

(The court reporter sought clarification.) 03:20:53

THE WITNESS: Sorry, a twisted pair Ethernet cable. You had to have what is called 03:20:53 03:20:53

a crossover cable, where a couple of wires were changed. Now since this is not necessary these days anymore because the network devices in computers basically test which kind of cable is being plugged in and then they automatically electronically change internally. 03:20:55 03:21:00 03:21:03 03:21:07 03:21:12 03:21:14

BY MR. BUROKER: 03:21:14

Q. But would a person of skill in the art in '96, as you've defined it, be able to look at this document and determine how to connect what's shown in Figure 7 directly to Figure 8? 03:21:19 03:21:22 03:21:26 03:21:29

MR. DAVIS: Objection to form. 03:21:34

THE WITNESS: From the level of disclosure in this document, I, as expert, cannot tell whether this is possible, so a person of ordinary skill in the art I doubt would be able to tell. You know one could try and see whether it worked. 03:21:40 03:21:45 03:21:47 03:21:49 03:21:51 03:21:53

BY MR. BUROKER: 03:21:56

Q. Okay, but you agree that Figure 9 shows an architecture in which the processor interface, which is the one shown in Figure 7, is connected via several routers to a bus interface which is what's shown in Figure 8? 03:21:57 03:22:02 03:22:06 03:22:12 03:22:18

A. That's correct. 03:22:21

Q. And the bus interface in Figure 9 could be a PCI bus interface, because that's one of the examples that the text tells us can be part of Figure 8, correct? 03:22:23 03:22:26 03:22:32 03:22:36
A. Correct, although in this case, SCSI is used as an example, yeah, there I agree. 03:22:38 03:22:42
Q. So if you were going to have a PCI bus interface in Figure 9 then you would connect it to one or more PCI devices and not one or more SCSI devices, right? 03:22:44 03:22:49 03:22:52 03:23:01
A. Yeah. 03:23:01
MR. BUROKER: SCSI is S-C-S-I, all caps. 03:23:02 03:23:02
THE COURT REPORTER: Thank you. 03:23:02
BY MR. BUROKER 03:23:02
Q. It's shorthand for -- what does "SCSI" stand for? 03:23:04 03:23:06
A. I believe "small computer system interface", but I wouldn't bet on it. This is a mass storage standard. 03:23:08 03:23:10 03:23:14
Q. Everybody just calls them SCSI. 03:23:21
A. Yeah. It's a byte-wide kind of bus. 03:23:24 03:23:30
Q. So with that in mind, if you have the Figure 7 RISC CPU, you place that in as 03:23:31 03:23:33

connected to the processor in Figure 9. You have 03:23:44
in mind what I'm talking about? 03:23:46
A. Yes, you're trying to replace the 03:23:48
top three -- top two boxes. 03:23:49
Q. Uh-huh. 03:23:52
A. One being CPU memory and the other 03:23:53
being processor interface with -- 03:23:55
Q. What's in Figure 7. 03:23:57
A. -- what's in Figure 7, yeah. 03:23:58
Q. So if you had that, and that RISC 03:24:00
CPU wanted to communicate to a PCI device in the 03:24:04
example where the bus interface is a PCI bus 03:24:09
interface and then, instead of SCSIs, you've got 03:24:12
a PCI device connection, correct? 03:24:15
A. Yeah. 03:24:17
Q. And in that situation then the bus 03:24:20
interface would be what's shown in Figure 8 as 03:24:28
the TNet bus interface and then the line would be 03:24:31
a PCI line and there would be a PCI device 03:24:36
connected to that? So you got that scenario in 03:24:42
mind? 03:24:45
A. (The witness nodded.) 03:24:45
Q. Okay. If this RISC CPU wanted to 03:24:46
do a write transaction to that PCI device -- 03:24:58
A. Uh-huh. 03:25:04

Q. -- what information would it send 03:25:06
to the processor interface? 03:25:09
MR. DAVIS: Objection; form. 03:25:13
THE WITNESS: With "processor 03:25:18
interface" you mean the system bus in Figure 7, 03:25:20
for instance, right? 03:25:23
BY MR. BUROKER: 03:25:24
Q. It would be the ... well, yeah, it 03:25:24
would be the system bus interface that is part of 03:25:30
the TNet processor interface in Figure 7, right. 03:25:33
That whole grey area is the TNet processor 03:25:39
interface according to this diagram. 03:25:44
A. Yeah, yeah, I understand that very 03:25:47
well. 03:25:48
Q. Right. 03:25:49
A. But here starts the problem. 03:25:50
First of all, in order for the processor to talk 03:25:53
to any particular device, the processor has to 03:25:57
know the physical address of that particular 03:26:02
device as seen from its own local address space, 03:26:06
right? The processor lives in its own address 03:26:15
space, which means potentially all one million 03:26:19
processors inside TNet live in their own 03:26:22
individual one million possibly different address 03:26:25
spaces because they don't all have to be the 03:26:26

same. So the fundamental question is what is the address of the particular PCI device connected to this TNet system, possibly having lots of such devices, as seen from the processor in this particular system at its particular system bus. Because the processor doesn't say, "I want to talk to the TNet interface", the processor says, "Here is an address" and then the rest of the system has to handle that. In order to get there, the PCI device first of all has to be initialized, right? When you switch it on it's dead, it says, "Leave me alone, I do not nothing but respond to PCI configuration cycles." Now, now this device has no way of directing any kind of PCI configuration cycles on the remote device of TNet. 03:26:29 03:26:33 03:26:39 03:26:44 03:26:48 03:26:52 03:26:55 03:26:59 03:27:01 03:27:05 03:27:10 03:27:13 03:27:15 03:27:19 03:27:22 03:27:25

Q. When you say "this device" you're pointing at what? 03:27:26 03:27:28

A. I'm pointing to the RISC CPU. 03:27:28

Q. Go ahead? 03:27:28

A. So for this to be initialized, which would be the first step prior to anything that could possibly happen, one has to understand how the people who developed that TNet-to-PCI interface conceived how this should happen. 03:27:33 03:27:36 03:27:38 03:27:40 03:27:45

There is no clear path to this solution, there are many possible solutions. One example would be, since you asked me as an expert in the field, is that this interface has a variety of particular configuration areas, and don't forget the RISC CPU in Figure 7 of the TNet reference has no way of generating a configuration cycle for that matter; it just does its own processor cycles, a completely different thing. Other bus, other bus states, other everything. So it would first of all know how to talk to the PCI interface on the TNet site. That would require the TNet system to be initialized, all the address translation tables to be initialized, all the nodes IDs of all nodes connected to TNet to be given a unique address, nothing it disclosed in here how this is possibly being done, and this is a highly complex problem, again because at this point in time there can only be one agent reasonably distributing those addresses, otherwise you have an address collision, very simple, which triggers the question who is the chosen one? There is a long paragraph about this complexity in the SCI standard if you want to read it.

So you have to initialize first the entire TNet system, set up all address translation tables, have to define address windows to reach the particular TNet nodes in this particular case because the PCI-to-TNet nodes have to be set up right. That would enable then the RISC CPU to communicate via read and write commands to the PCI-TNet interface, which would show up somewhere in the address space, in the physical address space of the RISC CPU in Figure 7. This is the first step. 03:29:16 03:29:19 03:29:21 03:29:23 03:29:30 03:29:36 03:29:39 03:29:44 03:29:47 03:29:50 03:29:54

Then the RISC CPU in Figure 7 would have to communicate with the PCI-TNet interface saying, "Actually I would like to do a PCI cycle". And to start with it would have to be a PCI configuration cycle and it would have to go through all possible slots available. And for every cycle it would get a response. Again there is many different ways. One way is, for example, that the particular PCI command is uploaded into the interface to some defined subaddress space and then by writing to some key address the interface executes now this PCI transaction and leaves the result in another register inside this ASIC, and then the processor comes back again, 03:29:56 03:30:00 03:30:03 03:30:06 03:30:08 03:30:11 03:30:18 03:30:21 03:30:23 03:30:27 03:30:31 03:30:34 03:30:37 03:30:40

reading this register saying, "What was the result of my command?" Right? So basically it would prepare the transaction that could be multiple write transactions to configure the device, and could also envision also solutions, but this is one example.

Now we have found there is a PCI device on that bus. The next step is run configuration cycles against the device to find out how much memory the device has in order to now map this in the context of the complete TNet address space and we have to keep in mind that the virtual addresses inside TNet have to be encoded on the -- have to be generated on the host site, so that the target device is properly received.

Once all of that has been done then there would be possibly a region in the address space of the RISC CPU, which would enable it to perform a write transaction which would then subsequently be captured by the TNet processor interface as shown in Figure 7. Now the CPU obviously knows the right addresses, it would then be translated by this TNet processor interface, the addresses would be converted into TNet addresses, this is a table lookup

particularly of this address translation logic shown in Figure 7 in the grey box. A packet would be generated, a TNet packet. There is some hint as to how the TNet packet looks like. The packet goes out, it percolates through the system, the routing devices know how to do this. At some point in time the packet is received by the PCI interface and then, if it's done right, one could implement something like that, and I have done this in the PCI-SCI adapter, except that the network is then SCI, that for a generic write executed by the CPU, an ordinary memory write of PCI would be executed. So one would basically allow a certain sub-functionality of PCI to be directly executed by the CPU for performance reasons, at the end of the day mostly will be probably reads and writes. All the other functionality is a complex initialization, configuration of these interfaces where the PCI interface here is not detailed. That would be part of the depacketizer functionality and a configuration space which is not explicitly shown. Every ASIC has a configuration space having this complexity. 03:32:13 03:32:18 03:32:20 03:32:24 03:32:27 03:32:30 03:32:33 03:32:35 03:32:39 03:32:43 03:32:47 03:32:53 03:32:58 03:33:02 03:33:05 03:33:08 03:33:10 03:33:14 03:33:18 03:33:23 03:33:27 03:33:35 03:33:37 03:33:40

So it's far from being simple. And I 03:33:41

should also say I mean nothing of what I have 03:33:44
just said is disclosed in this reference, I just 03:33:46
responded like I would do something like that or 03:33:51
some high-level person and we are far away from 03:33:54
an ordinary-skill-in-the-art kind of person here, 03:33:57
we are requiring system-level understanding of 03:34:00
highly complex multi-parallel systems. We 03:34:02
require the understanding routing algorithms and 03:34:05
network deadlock resolution. These are all very 03:34:11
complex subjects which have to be taken into 03:34:14
account, otherwise the system will simply not 03:34:20
work. 03:34:23

Q. Let me unpack that a bit, that was 03:34:28
a lot. 03:34:32

So looking at Figure 2, one of the 03:34:33
things that is shown under the PCI interface is 03:34:38
a PCI controller. 03:34:42

A. Yes. Bottom right. 03:34:45

Q. Is that a standard PCI device? 03:34:48

MR. DAVIS: Objection; form. 03:34:50

THE WITNESS: Again, I mean, this is 03:34:55
a very high-level diagram, but it does say "PCI 03:34:56
controller". And applying the definition we have 03:35:01
been using, although I mean this is not a patent 03:35:06
here, I would assume that if somebody uses the 03:35:09

words "PCI" -- which are well defined in industry -- then it's meant as a PCI as the PCI industry standard, and by that argument chain it would have to be a PCI-compliant device, correct.
BY MR. BUROKER:
Q. But does the term "controller" suggest that it is something different than a PCI device? Does the word "controller" mean anything to you in this context?
A. I mean, we're here at 10,000 meters flight height, right, trying to see little details. From this diagram I read we have a PCI interface connected to the network, TNet, and that means the primary path of communication here is the PCI interface connected to TNet. This is the particular ASIC we were discussing.
The PCI controller, why it's being called "controller" I don't know and I don't want to guess, but it is a device which is compliant to PCI and this is even further emphasized by showing that there is written "PCI" to this single line interconnecting these two devices which to me says this is a PCI bus, compliant PCI bus.
Q. So the PCI controller, you're not

familiar -- strike that. 03:36:51

Is there a thing in the PCI nomenclature of -- strike that. 03:36:53 03:37:01

Could this be a processor that operates to control all of the other devices on the PCI bus? 03:37:04 03:37:08 03:37:11

MR. DAVIS: Objection; form. 03:37:15

THE WITNESS: Other devices on this particular local PCI bus as shown in Figure 2? 03:37:22 03:37:24

BY MR. BUROKER: 03:37:32

Q. Yes. 03:37:32

A. PCI is a bus which allows multiple masters to operate, so from that point of view this could be almost anything, including a processor. 03:37:36 03:37:40 03:37:47 03:37:49

Q. And it would be possible that that processor is the one that does at least the initialization stage that you talked about for the other PCI devices, that wakes them up and gives them their addresses on that PCI bus? 03:37:51 03:37:54 03:38:00 03:38:02 03:38:06

MR. DAVIS: Objection; form. 03:38:11

THE WITNESS: This is highly constructed and from the -- I mean, this diagram is part of a paper written by a senior in the field, Robert Horst, he is Technical Director at 03:38:15 03:38:18 03:38:26 03:38:30

Tandem Labs, so obviously he has reached a relatively high level in his career and I would consider him an expert. 03:38:37 03:38:40 03:38:44

What they invented -- and they have quite a bit of discussion why they did that and what it is for -- was to develop TNet to enable a large number of computing devices, computer processors and memory -- and this is also indicated by the abstraction level here in Figure 2 where only CPU and memory is shown, not even any TNet interface -- to enable them to communicate very efficiently. 03:38:49 03:38:51 03:38:53 03:38:57 03:39:04 03:39:06 03:39:08 03:39:11 03:39:15

On top of that, of course such a large system has to have an interface to the outside world, otherwise it wouldn't make any sense, and for this reason all these additional devices, LAN controller, ATM controller, VME and PCI interfaces were created. To initialize such a highly complex system through a remote PCI interface to me would be taking the whole system upside down. What you would do is you would initialize the TNet system through the path for which you built it and that is the processors directly connected to it. There would have to be a mechanism to identify which is the one selected 03:39:17 03:39:19 03:39:22 03:39:25 03:39:34 03:39:37 03:39:42 03:39:45 03:39:50 03:39:52 03:39:55 03:39:58 03:40:00

to perform the first initialization, a large variety of different possible protocols possible, nothing disclosed here. And then the initialization would happen, and the PCI interface would be much more complicated if it would have to be built such that the configuration and this initialization could be done from the PCI side comfortably as well. I wouldn't do that at all as an expert. 03:40:06 03:40:11 03:40:14 03:40:17 03:40:19 03:40:23 03:40:25 03:40:27 03:40:30

BY MR. BUROKER: 03:40:30

Q. So, the same example I asked you about, if all of that were done, the initialization and so forth, then the flow that you describe just directionally would go from the RISC CPU through the TNet processor interface components? 03:40:34 03:40:42 03:40:47 03:40:52 03:40:56 03:41:01

A. Uh-huh. 03:41:03

Q. Next out onto the routers, one or more routers, until it reached the PCI bus interface that we've substituted for what's shown in Figure 9. 03:41:04 03:41:07 03:41:12 03:41:14

A. Uh-huh. 03:41:15

Q. And then the PCI bus interface would send it out on the PCI bus, something out on the PCI bus which would be received by the 03:41:16 03:41:18 03:41:24

appropriate PCI device; is that right? 03:41:28

MR. DAVIS: Objection; form. 03:41:30

THE WITNESS: After the proper initialization has been done, which I outlined, correct. 03:41:31 03:41:34 03:41:36

BY MR. BUROKER: 03:41:37

Q. And what you've said in your declaration was that until whatever information this is got to the PCI interface, it would not be a PCI bus transaction and the PCI bus transaction would be created at this PCI interface; is that correct? 03:41:37 03:41:38 03:41:41 03:41:46 03:41:50 03:41:53

A. That is correct, yes. 03:41:53

Q. Okay. So would you agree that in that situation the information received by the PCI interface would have to contain all of the information needed to create a PCI bus transaction? 03:41:55 03:41:58 03:42:03 03:42:07 03:42:13

MR. DAVIS: Objection; form. 03:42:14

BY MR. BUROKER: 03:42:18

Q. That information would need to be there in order for to create a PCI bus transaction, correct. 03:42:18 03:42:20 03:42:23

MR. DAVIS: Objection to form. 03:42:25

THE WITNESS: I mean I realize this is 03:42:29

a very complicated subject and the answer is not easy. I believe I understand where you're trying to get to but it's not that simple. 03:42:30 03:42:35 03:42:40

So, for example, we have to consider where we start and where we end, right? We start at the processor front side bus. And the processor has a certain set of functionality it can do. Most of that is cache coherency functionality which we absolutely don't care in the context of TNet even being put forward by Horst saying, "We don't need cache coherency in TNet" as opposed to SCI. There are 16 different PCI transactions possible. So the only thing that one can do or what people would try to do which I did in the PCI-SCI adapter for some performance, would be that if there is a certain write transaction arriving, what you get is an address, a virtual address in TNet land which is recognized by the PCI interface, translated to some other PCI address which has absolutely no relation to the physical address used by the processor at its front side bus, to then generate a pre-configured PCI transaction for this address range. So basically there is something prearranged saying, "Well if I write to this 03:42:43 03:42:47 03:42:50 03:42:54 03:42:59 03:43:02 03:43:04 03:43:08 03:43:11 03:43:15 03:43:21 03:43:24 03:43:28 03:43:31 03:43:35 03:43:37 03:43:42 03:43:47 03:43:51 03:43:56 03:44:00 03:44:04

address please do a memory write" or, "Please do a memory write multiple" or whatever other cycles one would have and that would have to be prearranged, could possibly even change over time. That makes this game even more complicated because usually it is very difficult to have multiple independent processors doing the same thing if you have a state, right? We call this a state because it has a context. And I'm trying to make it clear that you do not have, and you cannot have in this context, the complete information of the entire possible PCI context here in the far end as part of the network message going out. 03:44:06 03:44:09 03:44:13 03:44:16 03:44:18 03:44:22 03:44:24 03:44:28 03:44:30 03:44:34 03:44:36 03:44:40 03:44:45 03:44:49

BY MR. BUROKER: 03:44:49

Q. So, are you saying that it was not possible to build a PCI bus transaction in that it's just not possible to do because there's not enough information coming in from the CPU? 03:44:51 03:44:54 03:45:02 03:45:04

A. No, no. As I said, you have pre-configured interface here -- 03:45:07 03:45:10

Q. When you're saying "here" you're referring to -- 03:45:13 03:45:15

A. Yes, you're right, pre-configured interface, and I'm pointing to the right. 03:45:15 03:45:18

Q. The PCI interface box in Figure 2? 03:45:21
A. Correct. 03:45:25
Q. Go ahead. 03:45:27
A. Which instructs it to respond to certain TNet commands in a certain way. 03:45:28 03:45:32
Q. Okay. 03:45:35
A. Right? And obviously the instruction is, "Generate a particular PCI transaction upon this TNet command". But there is no PCI transaction then on TNet nor is there the PCI address on TNet. 03:45:36 03:45:40 03:45:43 03:45:46 03:45:52
Let me try to make it even -- show you the complexity at the example of a read transaction because that makes a couple of things even more obvious. 03:45:57 03:46:00 03:46:07 03:46:08
Q. Well, let me ask one question and then I'll let you do that. 03:46:09 03:46:11
What you're saying is that the PCI interface would take some information that it received through this flow from the CPU plus information it already had and then could compose a PCI bus transaction? 03:46:11 03:46:13 03:46:16 03:46:21 03:46:25
A. That is correct. 03:46:27
Q. Okay. So some but not all of the information needed to create a PCI bus 03:46:28 03:46:32

transaction would come through from the CPU down through that flow to the PCI interface? 03:46:34 03:46:38

A. For the given transaction. It would have to come through this flow via some other commands beforehand, yeah. 03:46:41 03:46:42 03:46:45

Q. All right. 03:46:47

A. Because the only path is here. 03:46:48

Q. Right. So Figure 5 shows some idea of the addressing format for a TNet transaction; is that correct? 03:46:51 03:47:07 03:47:11

A. Yes. 03:47:14

Q. Okay. So I used the example of a write request that would be from the CPU. So according to this the write request would have four sections: the header; the 4-byte TNet address, which is referred to as the A; the D box, which is zero to 64 bytes of data; and then C which is the 4-byte CRC, which is basically a hash, right? 03:47:15 03:47:18 03:47:24 03:47:26 03:47:31 03:47:36 03:47:40 03:47:45

A. It's an error correction. 03:47:47

Q. Error correction. 03:47:47

A. An error detection code, not correction, sorry, CRC cannot correct errors. 03:47:48 03:47:51

Q. Error detection code, right. So there are four pieces of information that would 03:47:55 03:47:57

be part of what the CPU in that situation would send down the pipe heading for the PCI, assuming everything has been initialized as you said, right? 03:47:58 03:48:00 03:48:07 03:48:10

A. Uh-huh. 03:48:11

Q. Why would you need both a destination ID, which is in the header, and a four-byte TNet address? Wouldn't the 20-bit destination ID be sufficient to identify where you wanted the packets of data to go on the TNet network? 03:48:21 03:48:23 03:48:29 03:48:33 03:48:37 03:48:42

MR. DAVIS: Objection; form. 03:48:43

THE WITNESS: The answer is no. This is a bit a question of semantics and how Horst chose to present this. And I mean this is a nice question because it nicely shows the fundamental difference between the two scenarios we have here. Now, I go to Figure 2, which I don't like because it's so abstract but now it helps. At the top you see three boxes saying "CPU" and "memory". 03:48:49 03:48:55 03:49:00 03:49:05 03:49:07 03:49:10 03:49:18 03:49:22 03:49:25

BY MR. BUROKER: 03:49:25

Q. Uh-huh. 03:49:26

A. And my leftover 16 gigabytes of memory, at that time one didn't have that much, 03:49:27 03:49:35

but 32 bits of address space is not that much for 03:49:37
a CPU today. Even at that time computers were 03:49:41
starting to have hundreds of megabytes of main 03:49:44
memory. So the address space needed to simply 03:49:47
address the memory, let alone to address anything 03:49:50
outside that CPU, like the entire TNet world, is 03:49:53
the address space the local CPU has and this 03:49:58
other 32 bits, okay? And, for example, let's say 03:50:01
the left CPU is CPU 1, the middle is 2 and the 03:50:09
right one is 3. If CPU 1 wanted to read 03:50:14
an address from CPU 3 it would have to say which 03:50:17
address, and that would be an address of the 03:50:19
entire possible address space of CPU 3. So in 03:50:22
this context there would be 32 bits. Of course, 03:50:26
all modulo address translation, but at the final 03:50:29
end, when everything is said and done, that would 03:50:34
have to be the correct physical address of that 03:50:36
particular address in CPU 3. 03:50:38

The same game I can play for CPU 2. And 03:50:41
in parallel computing this is exactly what 03:50:45
happens, right? You have many, many computers 03:50:46
which compute a certain piece and then somebody 03:50:48
has to go gather everything. But you still have 03:50:50
to be able to identify which processor you want 03:50:53
the data from, and that's what is considered the 03:50:55

node address or node ID. And if you send 03:50:58
a packet, the packet is always sent from somebody 03:51:05
to somebody and, since you expect an answer, the 03:51:07
packet has to contain the sender ID, otherwise 03:51:10
the return wouldn't possibly work. 03:51:13

So in the TNet world, the source of 03:51:16
destination address is necessary to identify the 03:51:21
individual devices, the nodes, and the 4-byte 03:51:25
TNet address is basically the -- sometimes it's 03:51:33
called subaddress space identifying the devices 03:51:34
inside a node. 03:51:38

For example, in SCI case the semantic 03:51:39
was chosen slightly different, one has said SCI 03:51:43
has a 64-bit address space and the upper 16 bits 03:51:47
by definition are the node ID and the rest 48 03:51:48
bits are local addresses. Whether or not you 03:51:54
separate that out and give them different fields, 03:51:57
is really just a detail. 03:52:00

Q. Right, isn't it possible, it says 03:52:03
that on page 5, the TNet address is a 32-bit 03:52:05
window into the destination's address space, 03:52:11
right? 03:52:14

A. Yes. 03:52:14

Q. So for a PCI device, that would be 03:52:15
the 32-bit address of the PCI device? 03:52:18

A. Not necessarily.

MR. DAVIS: Objection to form.

BY MR. BUROKER:

Q. But it could be. So that you could use the A field to fill in the PCI device address and use the header information to tell you where on the network that PCI device is found?

MR. DAVIS: Objection; form.

THE WITNESS: What you're referring to is one particular example of the address translation on the receiving node would be simple which doesn't mean the address translation on the sending node is trivial as well, because hardly ever the particular address you try to reach on the PCI subsegment would be available like that on the host node. It might be that there is just local memory, right? And you have to also take into account you have many possible devices which you want to connect to. For every of those devices you have to have an address window in the physical address space of the host CPU 1, 2 or 3. They can't be all at the same place, right? So already there you see that the address windows you have to have in the host CPU initiating the

transactions cannot map directly to the potential address windows needed on the target device, the PCI is only one example. 03:53:52 03:53:57 03:54:00

BY MR. BUROKER: 03:54:07

Q. What do you think that it means when it says that the TNet address is a 32-bit window into the destination's address space? 03:54:07 03:54:09 03:54:12

A. The destination address space could be more than 32 bits. 03:54:16 03:54:17

Q. How do you get that from the word "window", meaning that it's just a portion of the ... 03:54:25 03:54:26 03:54:30

A. This is a term of art, being used as that. So let's take this whole system as it would be built today, then this CPU has a 64-bit address space. And, let's say, I mean, the computers we have recently built have 256 gigabytes of memory, so obviously there is no way in this context with this TNet to address all 256 gigabytes. So in order for having a communication, one would have to restrict oneself to a 4-gigabyte sub-window in this huge address space which could be exposed to other nodes in TNet. But it may well be that every of these CPUs gets a different window based on the 03:54:31 03:54:33 03:54:38 03:54:44 03:54:49 03:54:54 03:54:56 03:55:00 03:55:07 03:55:10 03:55:14 03:55:18 03:55:22

address translation table in the TNet interface. 03:55:27

Q. So then this document also talks 03:55:36
about something called an "address validation and 03:55:38
translation table". 03:55:40

A. Yes. 03:55:42

Q. And that's described as being the 03:55:43
thing that would map the CPU's physical address 03:55:44
space to the virtual TNet address space, right? 03:55:47

A. Uh-huh. 03:55:51

Q. Okay. 03:55:52

A. Figure 7. Now, this thing has to 03:55:54
go both ways. And I mean, again, this is not 03:56:04
disclosed in here, but this is something I'm sure 03:56:09
Horst knows and also so do I, if you build 03:56:15
a system of that scale, this is what's being 03:56:18
called a shared memory system, right, or 03:56:22
a distributed memory system, allowing remote 03:56:27
direct access to the memory of other nodes inside 03:56:29
the system. When SCI was invented there was 03:56:33
a real war going on, very religious, as always, 03:56:38
between the distribute-shared-memory people and 03:56:43
the message-passing people. I mean these two 03:56:45
philosophies are maintained until today. So the 03:56:51
message-passing world says there is no 03:56:54
communication, direct communication to the local 03:56:58

memory of any other node, if you want to know 03:57:01
something you send a message saying, "Please tell 03:57:03
me what is stored there." And then the answer 03:57:05
comes back, usually requiring the processor to 03:57:07
actually actively respond. While the 03:57:09
shared-memory functionality says, "I grab 03:57:12
anything I just want." The caveat here is if you 03:57:14
have an error in any node, imagine you build 03:57:18
a system with a million processors -- I mean they 03:57:23
exist in the Blue Gene -- and one processor 03:57:26
starts writing funny nonsense to all sorts of 03:57:31
addresses on the remote nodes. Now you have 03:57:34
corrupted memory in another node and you have no 03:57:37
way of finding who caused it because no debugger 03:57:40
will possibly tell you that. That was the old 03:57:44
argument from the message-passing people against 03:57:46
the shared-memory people, saying, "You're 03:57:50
building a system which cannot be debugged." And 03:57:53
the shared-memory people said "Yeah, and your 03:57:55
message-passing interface is so slow we're ten 03:57:57
times faster." This is why there is more and 03:57:59
more, and this is here also indicated, access 03:58:03
protection built in, and this is why it's called 03:58:08
address validation, so access validation, so the 03:58:11
address translation tables in here basically 03:58:14

perform also the function of making sure that no unauthorized access to any other addresses inside the system is possible.

Q. So, let me just ask you some more questions about this flow we've been talking about. Is it your understanding that whatever packet that would be created by the CPU and passed through to the TNet processor interface, that then that information is transmitted on the physical layer, in other words over a cable, to the next hop in the system which I guess would be a router?

MR. DAVIS: Objection; form.

THE WITNESS: I have one problem with your question because you said whatever packet the CPU generated. The CPU does only memory transactions, the packets happen in the TNet processor interface. But aside from that ...

BY MR. BUROKER:

Q. So to be clear, some information is sent from the CPU and at the TNet processor a TNet packet is created and then it is placed on the physical layer for transmission to the router in Figure 9?

A. Yes.

Q. Okay.

A. And, I mean, one example of the physical interface of TNet is Figure 4.

Q. Figure 4, right. And Figure 4 shows transmission over a cable that's used in ECL?

A. Yeah.

Q. Right? ECL I guess it's called?

A. Yes.

Q. And do you agree with Mr. Young that that is a form of low-voltage differential signalling? Not the industry standard LVDS but a form of low-voltage differential signalling?

A. The inventors of LVDS would now yell and scream because LVDS was invented to do away with ECL. ECL was the way signals were communicated -- it's a differential standard, too -- if things had to be fast. But ECL has been extremely power hungry and usually is defined on negative voltages which is the last thing you really want in low-voltage ASICs these days. It's a current signal, as it says, emitter-coupled logic. The emitter drains basically the current onto the cable. Voltages only happen based on the termination scheme. I'm

not sure whether or not ECL is really 04:01:36
an established standard such as the IEEE 1596.3. 04:01:39
At 50,000 meters flight height one might say 04:01:48
there is certain similarities, but low-voltage 04:01:52
differential signalling, in particular the 04:01:56
original LVDS standard, was created to avoid ECL. 04:01:58
So I would not consider this in the broader 04:02:04
context. Now, if you say this is a differential 04:02:08
signal that is certainly correct. 04:02:13

Q. Right, and it is differential 04:02:16
signalling you agree with that? 04:02:20

A. Absolutely, yes. 04:02:21

Q. Okay. The question is whether 04:02:22
it's low voltage or not I guess is the issue, 04:02:26
right? 04:02:29

A. Yeah. 04:02:32

Q. And you say LVDS was a well-known 04:02:39
improvement over ECL for low-voltage differential 04:02:44
signalling? 04:02:48

A. LVDS is a big improvement over 04:02:49
ECL. As you can see ECL doesn't exist anymore. 04:02:53
I mean these computers all use LVDS, for 04:02:55
instance, to talk to the graphics display which 04:02:58
is by far the fastest, probably the fastest 04:03:00
connection inside laptop computers. I was 04:03:05

pointing to a laptop computer. ECL, for it being 04:03:09
so very power hungry and for all the other 04:03:14
disadvantages I just quoted, is, in this context, 04:03:17
not being used. 04:03:20

Q. This figure shows the information 04:03:26
the TNet packet going through an 8B/9B encoder. 04:03:31

A. Yeah. 04:03:38

Q. Do you agree that that is a form 04:03:39
of encoding that meets the claim -- strike 04:03:41
that -- that meets the term in the claim 24 of 04:03:46
the '814 Patent? 04:03:49

A. It is one form of encoding and it 04:03:55
does fit the definition of encoding which I set 04:03:57
forth but it is not the particular incarnation of 04:04:00
encoding which has been used in this patent. 04:04:03

Q. Right, but if something uses -- is 04:04:05
it 8-bit/9-bit or 8-byte/9-byte? 04:04:09

A. Bit, 8-bit/9-bit encoder. 04:04:12

Q. Normally capital B mean byte. 04:04:13
It's confusing. 04:04:17

So if somebody is using 8-bit/9-bit 04:04:18
encoding then that would be the kind of encoding 04:04:22
that is contemplated in claim 24 of the '814 04:04:26
Patent, right? 04:04:31

A. If you would have said this is 04:04:41

a kind of encoding according to the definition I 04:04:43
set forth, yes. 04:04:45

Q. Okay. 04:04:46

A. Now, I mean, to be honest, I mean, 04:04:47
since I'm under oath and I'm trying to be really 04:04:51
as accurate as I can possibly be, my 04:04:54
understanding is these terms, as they are 04:04:56
construed in the patent, have to be seen in the 04:04:58
light of the patent document. This patent 04:05:01
document doesn't discuss 8B/10B encoding or 8B/9B 04:05:05
encoding or 4B/5B encoding, these are the typical 04:05:11
standards. In fact 8B/9B is not very common. 04:05:16
And since you specifically asked for claim 24 04:05:19
this is now a detail of patent law I'm not 100 04:05:23
percent sure how to answer. 04:05:27

Q. Okay. You agree though that 04:05:29
what's shown in Figure 4 is a serial transmission 04:05:43
of data between what says "Cabinet B" and 04:05:47
"Cabinet A"? 04:05:51

MR. DAVIS: Objection to form. 04:05:52

THE WITNESS: If we go to the 04:05:56
definition I put forth for what is serial -- and 04:05:58
we looked at that already so I don't want to 04:06:01
repeat it -- but it basically says if a certain 04:06:03
amount of information is transmitted over 04:06:07

a smaller number of signals, then taking into account that processors at the time -- where this was published at the time when the patents were filed -- were typically 32 bits or more, then it is consistent to be a serial transmission, right? 8 bits aren't much less than 32.

BY MR. BUROKER:

Q. So let me ask you then, the flow of data we've been talking about, looking at Figure 8, the TNet packet would come in and be received at the TNet interface and be stored in -- a packet buffer's just something to store things while other packets are being processed; is that right?

MR. DAVIS: Objection; form.

THE WITNESS: What really happens inside these packet buffers depends on a lot of things which are not disclosed in here. So, for example, if TNet would -- I don't remember the clock rate, whether there are any clock rates specified here, what is the transmission speed of TNet -- but if TNet would be much faster than the particular bus interface here, such as PCI, then it could happen that this interface cannot work off the packets at the speeds being arrived.

Then there is typically what one 04:08:28
implements, so-called derandomizing buffers, to 04:08:32
basically absorb a burst of writes. Of course 04:08:36
that can only be done to a certain extent and in 04:08:40
fact the size of such buffers has been always 04:08:43
a long debate where lots of simulations are being 04:08:46
done to find an optimum, because if you put in 04:08:49
too much it just costs money and it's never being 04:08:51
used and if you put in too little you introduce 04:08:54
a lot of flow control on the network saying, 04:08:56
"Wait, wait, wait, wait, can't do any more, 04:08:59
slowing things down" and so forth. 04:09:01

The second reason for the packet 04:09:03
buffers is once the packet is being received, 04:09:06
there needs to be a decoding done, it needs to be 04:09:08
understood what particular transaction should 04:09:11
result from that, then the interface, once it 04:09:13
recognized okay, "I need to do this transaction", 04:09:16
it needs to acquire the PCI bus, so there has to 04:09:19
go out a PCI bus request, a bus arbiter has to 04:09:23
say, "You can" or, "You have to wait". When it 04:09:26
says, "Bus granted, you can use the bus", it 04:09:28
still has to wait for any possibly still ongoing 04:09:30
bus transaction to finish. So these are random 04:09:33
times causing delays, random delays. And only 04:09:36

after all of that has happened then the PCI 04:09:39
transaction can happen, and then only the data 04:09:42
which is starting to be accumulated here can be 04:09:45
drained. 04:09:50
So a rule of thumb is the minimum size 04:09:51
of such a packet buffer would be the maximum 04:09:55
packet size which could be received because 04:09:57
otherwise you would risk losing data coming in 04:10:01
and the buffer being full. 04:10:04
BY MR. BUROKER: 04:10:04
Q. So out of the buffer would be some 04:10:08
information that would be depacketized. At what 04:10:12
point in this were you contemplating that the PCI 04:10:15
bus transaction would be generated? 04:10:19
A. I mean that would have to happen 04:10:26
in the bus interface, or I would put it into the 04:10:28
context of the bus interface. 04:10:32
Q. Yeah, but of these boxes in the 04:10:34
bus interface, where would that take place? Oh, 04:10:35
the one that just says "bus interface"? The long 04:10:39
box that says "bus interface" -- 04:10:42
A. Exactly. 04:10:45
Q. -- within the square that says 04:10:46
"TNet bus interface"? 04:10:47
A. I mean, yeah. What you have here 04:10:48

is, again, there's just so many details which are implicit here but not obvious and not really shown. But if you look at the TNet link, this has got to be something running at relatively high clock rates. You have PCI on the other side, comparably slow clock rates. What comes in is byte write, right? I mean 9 bits but it's basically bytes in one or the other form, as outlined in the document here basically ... where is it? Yes, in fact, it's not explicitly in here at all. But obviously it can't be more than 9 bits. In fact, no, it can only be 8 bits because it's an 8B/9B encoder and PCI is at least 32 bits, so this whole thing has to be expanded, which is the functionality of the depacketizer. So you have a TNet interface with a rather high clock rate going into the packet buffers, and then the context depacketizer suggests that here the unframing is done, the word width is recreated. The packetizer would probably try to extract already the addresses and separate them from the data, create nice 32-bit data word chunks and so forth, and then the bus interface would have to know what to do with this kind of thing. And again Figure 8, of course, has to

have all the functionality in there that is also shown in Figure 7. So we, again, have address validation, translation, access control, the whole nine yards, which is not shown here at all. This is not something I would put as sub-functionality of the bus interface. In fact, I don't know where I would put this. I would say this is just missing here as abstracted away now.

Q. But under that scenario, if a PCI bus transaction was created, it would be then sent on the PCI bus to be received by the PCI device to which it was addressed, right?

A. Correct.

MR. DAVIS: Objection to form.

BY MR. BUROKER:

Q. For that PCI device to act on the transaction, whatever the transaction is?

A. (The witness nodded.)

Q. Right? So, would you agree at a minimum that in that scenario the CPU has transmitted information that was used to create a PCI bus transaction?

MR. DAVIS: Objection; form.

THE WITNESS: Could you define "information that was used" a little bit more

specific? 04:14:17

BY MR. BUROKER: 04:14:17

Q. I'm trying to use in its broadest sense, not trying to call it data, not trying to call it address bits, just saying if the CPU sent information that was received by and interpreted by a PCI bus device? 04:14:18 04:14:21 04:14:23 04:14:26 04:14:36

MR. DAVIS: Objection; form. 04:14:39

THE WITNESS: The problem why I'm hesitant to answer is there is some information sent by the CPU which finally results in the PCI transaction which, however, requires additional other information which has to be set up earlier in the context of everything, thereby the information all by itself is not sufficient to create such a PCI transaction. Therefore I'm not sure whether I should say yes. 04:14:43 04:14:45 04:14:49 04:14:53 04:14:55 04:14:58 04:15:01 04:15:04 04:15:07

BY MR. BUROKER: 04:15:12

Q. And one of the reasons why you say that Horst doesn't disclose everything in, for example, claims 24 and 31, is that there is no northbridge or peripheral bridge to communicate all of the pieces of information of a PCI bus transaction in serial form, right? 04:15:12 04:15:13 04:15:18 04:15:23 04:15:28 04:15:31

MR. DAVIS: Objection; form. 04:15:35

BY MR. BUROKER: 04:15:36

Q. That's one of the opinions you offer. Like the header on page 85 of your '814 declaration. 04:15:37 04:15:40 04:15:47

MR. DAVIS: Objection; form. 04:15:56

THE WITNESS: I mean I do stand by what I wrote in my report. 04:15:58 04:15:59

BY MR. BUROKER: 04:16:01

Q. And that's because no matter what it's your view that what's transmitted over the TNet network are TNet packets. That's the second sentence of paragraph 129, right? 04:16:02 04:16:07 04:16:10 04:16:13

A. Yeah. 04:16:18

Q. And it's your view that the TNet packets don't have all of the information to compose a PCI transaction and, therefore, the entire PCI bus transaction is not sent as part of the TNet packet, right? 04:16:19 04:16:23 04:16:27 04:16:34 04:16:36

MR. DAVIS: Objection; form. 04:16:37

THE WITNESS: I mean in Horst, because you say the entire PCI transaction is not sent over the TNet, that would suggest that there is a PCI bus here having PCI transactions. There is no PCI transaction anywhere in this whole architecture except for the far end inside the 04:16:46 04:16:47 04:16:50 04:16:52 04:16:57 04:17:00

controller. And I'm really happy to discuss this further but could have a short break now? 04:17:03 04:17:06

MR. BUROKER: Sure, we'll go off the record. 04:17:11 04:17:13

(Brief recess taken 4:17 p.m. - 4:27 p.m.) 04:17:13

BY MR. BUROKER: 04:27:10

Q. So let's talk about that same configuration we've been talking about, but where the PCI device wants to communicate with the CPU and, you know, all the caveats you had earlier about how it had to be configured and all that sort of stuff. But in that case the PCI device would originate a PCI transaction up the PCI bus, right? 04:27:14 04:27:20 04:27:22 04:27:31 04:27:35 04:27:38 04:27:41 04:27:45

A. Of course, there is no other way. 04:27:46

Q. And that would then get routed to the PCI bus interface that's shown in Figure 2 and that we, you know, assume looks something like what's in Figure 8, right? 04:27:51 04:27:54 04:28:06 04:28:08

A. Yes, but before we go further -- 04:28:14

Q. Oh, I'm sorry, that's not right. So the PCI device would communicate and that would go to the PCI bus interface which would connect to a TNet bus interface or would it be a TNet PCI bus interface? I'm confused. 04:28:16 04:28:18 04:28:20 04:28:25 04:28:31

MR. DAVIS: Objection; form. 04:28:36
THE WITNESS: Yeah, I mean, according 04:28:37
what we discussed earlier I would say, if we look 04:28:39
at Figure 8, this is the PCI bus and that would 04:28:42
interface through this interface to TNet as 04:28:47
a system with everything. And what happens at 04:28:50
the far end then depends what target node is 04:28:53
being addressed. But before we go into details 04:28:56
I would like to know are we talking now read 04:28:59
transaction, write transaction, what transaction? 04:29:03
BY MR. BUROKER: 04:29:06
Q. I think I said, but let me 04:29:06
clarify, a write transaction. So the PCI wants 04:29:07
to write something into the memory associated 04:29:09
with one of the remote CPUs shown in Figure 9. 04:29:12
A. Uh-huh. 04:29:25
Q. Right? So it would start with 04:29:26
a PCI bus transaction of a write command type, it 04:29:28
would be transmitted on the PCI bus, right? 04:29:33
A. Yeah. 04:29:37
Q. That would end up at the PCI bus 04:29:38
interface which would then create a TNet packet, 04:29:42
correct? 04:29:48
A. No. 04:29:49
Q. What's wrong with what I said? 04:29:51

A. It would create one or multiple TNet packets because PCI bus transactions can have a certain length and they can certainly have more than 64 bytes being transmitted, that really depends on what device you have. So, for example, in here you have disks connected, there could be a PCI rate controller having a disk and disk blocks are 512 bytes. But TNet, referring to Figure 5, allows only zero to 64 bytes of data. That means if there is a longer ongoing PCI transaction that would result in multiple TNet packets being generated, whatever size packets then will depend on the detailed configuration, but there is no one-to-one relationship between a TNet packet and a bus transaction, on either side be it a processor or be it PCI. 04:29:53 04:29:56 04:29:59 04:30:02 04:30:06 04:30:09 04:30:14 04:30:17 04:30:22 04:30:28 04:30:32 04:30:34 04:30:39 04:30:42 04:30:44 04:30:46 04:30:49

Q. Right, but the data would be the same. The data of a PCI bus transaction that is of a write command would go directly into the data field of a TNet packet, correct? 04:30:50 04:30:51 04:30:56 04:31:01

MR. DAVIS: Objection to form. 04:31:07

THE WITNESS: It would be at the -- 04:31:10

THE COURT REPORTER: I didn't get the last word of the answer sorry, you were all three 04:31:16 04:31:16

speaking at the one time. You said, "It would be at the ..."?

BY MR. BUROKER:

Q. I'll just start over.

So the data of a PCI transaction of a write command variety, would then be filled in to the data portion of a TNet packet, correct?

MR. DAVIS: Objection; form.

THE WITNESS: The data would go through the 8B/10B encoder as shown in Figure 4, but you can also nicely see the decoder to it to complete the symmetry. And on TNet there would be an encoded version of it. The data would be physically different but it could be recreated then by the 9B/8B decoder.

BY MR. BUROKER:

Q. And let's just say my write transaction I'm talking about a small amount of data, less than 64 bytes, then there would be one TNet packet that would need to be encoded to be transmitted over the TNet links, right?

MR. DAVIS: Objection to form.

THE WITNESS: I assume so. This is one way it could be done, yeah. The reason why I'm a bit careful here is the following. There are

often alignment requirements on data as to be put 04:32:44
into packets. That means if you have a 32-byte 04:32:48
write you want to do but it starts off at an odd 04:32:57
address starting at address offset, say, 47, 04:33:02
which means the 32 bytes align 32-byte blocks. 04:33:05
It often happens that two network packets are 04:33:10
being created for efficiency reasons. This 04:33:12
really depends on lots of details how these 04:33:16
interfaces are implemented. There is no clear 04:33:21
indication in this document how it is being done, 04:33:26
but this is something which happens a lot. 04:33:29
BY MR. BUROKER: 04:33:29
Q. A simple form would be to take 04:33:31
just the data out of the PCI bus transaction and 04:33:33
fill it into the data component of the TNet 04:33:37
transaction and if there's any leftover space 04:33:43
just pad it with zeros, right? That's one way to 04:33:46
do it? 04:33:49
MR. DAVIS: Objection; form. 04:33:50
THE WITNESS: You can't pad with zeros, 04:33:54
because it would mean you write more data 04:33:57
which -- 04:33:59
BY MR. BUROKER: 04:33:59
Q. Well, it's -- 04:34:00
A. And you don't have to, because the 04:34:01

TNet packet has a length word which allows it to 04:34:07
be of variable length. But the padding is being 04:34:11
done in case of other networks which have 04:34:15
fixed-length packets where basically zeros are 04:34:17
being padded but then there is still an indicator 04:34:21
which of the bytes are actually valid. 04:34:25

Q. Forget what I said. A simple form 04:34:29
of transmission of the data would be to just take 04:34:32
the data from the PCI bus transaction, fill it 04:34:35
into the data field and then set the data link to 04:34:38
indicate the exact length of that data from the 04:34:45
bus transaction? 04:34:48

MR. DAVIS: Objection to form. 04:34:49

THE WITNESS: And this is one possible 04:34:50
way it can be done, yet it's not disclosed here 04:34:56
in particular. 04:34:59

BY MR. BUROKER: 04:35:02

Q. And what is why your view about 04:35:05
what would happen to the other pieces of the PCI 04:35:07
bus transaction as part of the process to create 04:35:10
the TNet packet? 04:35:19

MR. DAVIS: Objection; form. 04:35:22

THE WITNESS: What do you mean with the 04:35:23
other portions? 04:35:24

BY MR. BUROKER: 04:35:27

Q. So the address, the command, the control line and the byte enables, the other things. You know there's 47 bits that we talked about on the PCI bus transaction, what happens to the rest of those bits of data? 04:35:27 04:35:29 04:35:32 04:35:36 04:35:38

MR. DAVIS: Objection; form. 04:35:42

THE WITNESS: I would expect the TNet interface not to respond to all -- or not to transform all the particular PCI commands into TNet functionalities. So, for example, I wouldn't say any way to, for instance, do a PCI configuration cycle for TNet, right? 04:35:47 04:35:50 04:35:56 04:36:01 04:36:06 04:36:10

What we are doing here is we're jumping forth and back between a higher abstraction layer and more transaction and physical layer inside these buses and that can cause confusion, therefore I would like to be really careful. 04:36:14 04:36:16 04:36:21 04:36:24 04:36:26

There is the class of read transactions, there is the class of write transactions and there is a whole subclass of read transactions which is in PCI defined as a read configuration, read I/O, read memory. In case of a processor you have yet another set of kinds of reads, the entire span of cache coherency protocols which are all flavors of 04:36:30 04:36:32 04:36:34 04:36:36 04:36:39 04:36:46 04:36:50 04:36:56

reads. TNet just can do a read, nothing else. So all the other functionality behind is gone inside TNet and has to be, if needed, recreated by some auxiliary infrastructure we already discussed. 04:36:58 04:37:05 04:37:11 04:37:14 04:37:18

So, in this case, I would expect the interface between PCI and TNet to be configured after everything is initialized to basically respond to memory reads and memory writes. That would be the easiest thing, and that would be the context in which I expect this document to be written namely having an I/O device, being PCI, which has produced some data, which it wants to deliver to some CPU, and in this context we don't need to understand the difference between a read, a read multiple, or a write line or whatever, we don't need to understand cache coherency, we just need that data to find its way all the way through the system to the far end, to the memory, right? But there is no one-to-one correlation between any given PCI transaction and any given TNet packet. 04:37:19 04:37:22 04:37:25 04:37:28 04:37:31 04:37:35 04:37:39 04:37:46 04:37:49 04:37:53 04:37:55 04:37:57 04:38:00 04:38:02 04:38:05 04:38:11 04:38:13

And, I mean, I understand this is it important and I think it becomes really, really clear if you take a read transaction, because 04:38:17 04:38:18 04:38:23

writes can be posted, reads cannot. 04:38:27

BY MR. BUROKER: 04:38:27

Q. But to continue what we were talking about, a write PCI bus transaction is sent and the TNet interface, the TNet-PCI interface creates one or more TNet packet that gets sent over the same set of components, the routers and so forth, and they end up at the processor interface associated with the correct CPU, correct? 04:38:31 04:38:33 04:38:43 04:38:49 04:38:54 04:38:59 04:39:03 04:39:08

A. Provided all the translation tables, everything is initialized properly, yeah. 04:39:09 04:39:11

Q. Okay. And so then that processor interface, the TNet processor interface, would then pass the TNet packet, it would create whatever form of bus transaction the CPU was expecting, right? 04:39:14 04:39:17 04:39:20 04:39:31 04:39:34

MR. DAVIS: Objection to form. 04:39:37

BY MR. BUROKER: 04:39:40

Q. Looking at Figure 7 in that line between the TNet processor facing the RISC CPU, for example, there would be some interface that would create perhaps a CPU bus transaction, right? 04:39:40 04:39:42 04:39:47 04:39:50 04:39:54

A. This figure, to me, isn't 04:39:56

perfectly clear. If I take this figure and one has to be really careful with these very high level figures, but if I take this figure and take it literally, we could say if there is a write transaction arriving at the TNet link there is absolutely no need to bother the CPU on the system bus, because that ASIC here -- sorry, this TNet processor interface, which I assume to be an ASIC because it has to be quite fast, has a direct memory interface, even part of this design block, so it could perform the write transaction directly to the memory without bothering the CPU. So, in an extreme case, there could be a write transaction coming in, being executed against the memory by the CPU, execute another transaction against TNet to some other address sending a network packet out, because network is able to submit and receive simultaneously. 04:39:59–04:40:52

However -- and this is the reason why I'm puzzled, this is bad style -- because that means the snooping functionality of that RISC CPU -- 04:40:53–04:40:58

Q. The what kind of functionality? 04:41:05

A. Snooping, like Snoopy. 04:41:07

Q. Okay, that's what I thought you 04:41:08
said but I wanted to make sure. 04:41:09
A. This is a term of art, believe it 04:41:11
or not, and it really comes from Snoopy being 04:41:13
very nosy. 04:41:16
Q. So the snooping functionality. 04:41:24
A. It means the following. These 04:41:27
CPUs, and I've shown you all of them have caches, 04:41:30
and if you have data in a cache and somebody else 04:41:33
writes to memory, it can happen that the data 04:41:40
written to is the data of which you have a cached 04:41:44
copy. Yeah? 04:41:48
Q. Right. 04:41:50
A. If that happens, aside from the 04:41:50
CPU without the CPU knowing, you have what we 04:41:53
call a stale copy. And if you have a system 04:41:55
which allows you to have a stale copy of a cache, 04:42:00
you have created a computer which is not working, 04:42:02
or you have to do a whole lot in software on top 04:42:08
of that. The only remedy to this problem would 04:42:12
be that every time you try to read something from 04:42:15
an area where you suspect somebody could have 04:42:18
possibly written, meaning you have an enabled 04:42:22
remote access to that region, you have to flush 04:42:24
the caches. Now, flushing caches is something 04:42:27

extremely expensive you really don't want to do. So this is why processors have a functionality, they basically watch what is happening on the bus. Like somebody else comes in, writes to the memory, the processor says, "Wait a minute I want to see what you're doing here." Then it compares the physical addresses on that bus, and if then there is a match to a cache line being hit, either the cache line is being invalided as safe or, even fancier, the processor -- sorry the cache does that, looks what is the data being transmitted and copies it simultaneously while it goes from memory into the cache line and then you still have a coherent cache line, yeah? And caches were well known at that time and were very important already. So this figure here certainly leaves something out or doesn't mention something which would be quite useful to have. 04:42:30 04:42:33 04:42:36 04:42:38 04:42:41 04:42:43 04:42:45 04:42:47 04:42:50 04:42:54 04:42:59 04:43:01 04:43:03 04:43:05 04:43:13 04:43:16 04:43:18 04:43:20

Q. Well at a minimum the CPU would be connected to the main memory through something other than the TNet processor interface, right? 04:43:22 04:43:24 04:43:27

MR. DAVIS: Objection; form. 04:43:30

THE WITNESS: I mean the way it's drawn here has some deficiencies. 04:43:32 04:43:34

BY MR. BUROKER:

Q. But in like Figure 2 it shows them like connected --

A. Yeah, but this is so abstract in a way --

Q. -- or drawn together, right?

A. But in Figure 2 the memory talks directly to the TNet and this is obviously not happening. 04:43:46 04:43:48 04:43:51

Q. Okay, so in that situation, somehow or another the TNet processor link has taken the packet created a transaction to write the data that came from our PCI bus device into memory. 04:44:00 04:44:04 04:44:09 04:44:15 04:44:21

A. Uh-huh. 04:44:22

Q. Right? 04:44:23

MR. DAVIS: Objection; form. 04:44:23

BY MR. BUROKER: 04:44:27

Q. So is it fair to say that the CPU main memory components received PCI bus transaction information or not? 04:44:28 04:44:33 04:44:40

MR. DAVIS: Objection; form. 04:44:42

THE WITNESS: They received the payload of a PCI write, they did not receive a PCI transaction, it's not there anymore, it's something else. 04:44:43 04:44:47 04:44:54 04:44:59

BY MR. BUROKER: 04:44:59

Q. And when would you say the PCI bus transaction in that flow ceased to exist? 04:45:00 04:45:03

A. Exactly at the moment where it leaves the PCI to TNet interface. In the very moment where the packetizing starts to happen, we have something else. For it to continue to exist one would have to be able to show that all the states and functionality defined in here would have to still be present. 04:45:08 04:45:10 04:45:15 04:45:18 04:45:24 04:45:27 04:45:30

Q. And that's based on your understanding of the TNet -- strike that -- of the term "PCI bus transaction". Would you agree if a broader interpretation of PCI bus transaction was adopted by the PTAB here, which just required some of the information from a PCI bus transaction, that in that definition the CPU memory elements have received at least a portion of the PCI bus transaction, the payload? 04:45:32 04:45:33 04:45:35 04:45:40 04:45:43 04:45:51 04:45:53 04:46:02 04:46:04

MR. DAVIS: Objection; form. 04:46:07

THE WITNESS: I'm not aware of such a definition. 04:46:09 04:46:10

BY MR. BUROKER: 04:46:12

Q. I'm just saying -- and this is a hypothetical -- if they were to adopt it, would 04:46:12 04:46:14

you agree that at least you said the payload would be received; is that correct?

MR. DAVIS: Objection; form.

THE WITNESS: These what-if discussions are dangerous because they are highly hypothetical. In that case I would like to review the exact wording of the adopted definition, then I would like to take my time and really verify this against the patent claims and the entire prior art cited in order to give a competent answer. But upon some very generic I think this is quite difficult. And, second, I would have a problem because you cannot talk about a standard and then say we just take part of it because then it's not a standard anymore. I mean, this is the fundamental principle of the definition of such a thing. You have to have the complete functionality or it won't work.

BY MR. BUROKER:

Q. Right, well, but claim 24 never identifies a PCI device that has to use that information, right?

MR. DAVIS: Objection to form.

THE WITNESS: There is no PCI device explicitly mentioned in claim 24, yet --

BY MR. BUROKER: 04:47:45

Q. Of the '814 Patent? 04:47:46

A. Of the 814 Patent, correct. 04:47:48

Q. Right. 04:47:50

A. Yet a PCI transaction is executed in order to communicate with the PCI device, nothing else makes any sense. So this is implicitly clearly stated here. It's implicitly included so I should say. 04:47:50 04:47:54 04:47:57 04:47:59 04:48:05

Q. But it's not explicitly included? 04:48:05

A. Sorry, I misspoke. I am sorry, it's implicitly included. 04:48:12 04:48:14

Q. But based on what? Just because it uses the word "PCI bus transaction" you're saying implicitly it requires that there be a PCI bus device to be able to receive and process it? 04:48:16 04:48:18 04:48:22 04:48:26

MR. DAVIS: Objection; form. 04:48:27

THE WITNESS: For what other reason would you execute a PCI transaction? 04:48:29 04:48:30

BY MR. BUROKER: 04:48:31

Q. Well, it doesn't say you execute a PCI transaction. 04:48:31 04:48:33

MR. DAVIS: Objection; form. 04:48:34

BY MR. BUROKER: 04:48:36

Q. Does it? 04:48:36

A. "... the north bridge to communicate address and data bits of a PCI transaction in serial form ..." 04:48:43 04:48:43 04:48:50

-- going on further and further. What would the purpose be to communicate a PCI transaction somewhere unless one wanted to execute such PCI transaction? 04:48:50 04:48:52 04:48:58 04:49:00

Q. I don't know. It's one of the -- the claim doesn't say that you have to execute a PCI bus transaction, correct? 04:49:01 04:49:03 04:49:05

MR. DAVIS: Objection; form. 04:49:10

BY MR. BUROKER: 04:49:12

Q. Claim 24 of the '814 Patent. 04:49:12

A. Well, if you read the patent it's quite obvious it's stated in here. 04:49:15 04:49:17

Q. Right, but your job and the PTAB's job is to compare what's in the claim to the prior art. So claim 24 doesn't explicitly say that a PCI bus transaction has to be executed, correct? 04:49:20 04:49:23 04:49:27 04:49:29 04:49:33

MR. DAVIS: Objection; form. 04:49:36

THE WITNESS: I mean I believe I already answered. I believe it is implicitly included, but it's not explicitly stated, yes. 04:49:47 04:49:48 04:49:50

BY MR. BUROKER: 04:49:50

Q. So is that part of the interpretation of claim 24 that you used in looking at the prior art? You were looking to make sure that the prior art actually executed PCI bus transactions that are communicated from the northbridge? 04:49:56 04:49:57 04:49:58 04:50:00 04:50:03 04:50:07

MR. DAVIS: Objection; form. 04:50:09

THE WITNESS: No, I mean I have outlined how I looked at these claims, and the discussion we conduct is whether or not there is an encoded -- I mean one of the areas we're discussing here, aside from the other functionality such as address translation and coding, were whether or not there were encoded PCI transactions on the discussed network, which are in the two references SCI and TNet. 04:50:13 04:50:15 04:50:18 04:50:22 04:50:25 04:50:28 04:50:32 04:50:34 04:50:37

BY MR. BUROKER: 04:50:37

Q. Right. And then is your opinion also the same that having a PCI bus transaction that can be executed is implicitly required by claim 31 of the '814 Patent and claim 54 of the '873 Patent? 04:50:43 04:50:45 04:50:51 04:50:54 04:51:03

MR. DAVIS: Objection; form. 04:51:06

THE WITNESS: I mean in the context of PCI transaction it clearly says: 04:51:20 04:51:21

"... a peripheral bridge coupled to said microprocessor unit without any intervening Peripheral Component Interconnect (PCI) bus, said peripheral bridge coupled to second LVDS channel to communicate address and data bits of PCI bus transaction in serial form over said second ... channel."

And this is what I used to evaluate.

BY MR. BUROKER:

Q. But if the peripheral bridge in chamber 31 transmits the PCI bus transaction that never gets received and never gets executed as a result, is it your understanding that the claim has been met or not met?

A. It strict sense it has been met, but it wouldn't make any sense to build a system like that. And you would be hard pressed to find one.

Q. Well, you'd find one where the PCI device was broken and didn't receive the transaction, it would still have been sent, right?

MR. DAVIS: Objection; form.

BY MR. BUROKER:

Q. So there are circumstances in

which a device may send a PCI bus transaction to a device and nothing happens because that device is broken. 04:52:29 04:52:32 04:52:35

A. Yeah, but this would be a highly constructed special case and the system was still built to communicate between this host and the PCI device and, in such an exceptional case, a transaction would fail but it would still be legitimate transaction on the bus, it would time out, and be responded to as an error. 04:52:40 04:52:43 04:52:46 04:52:49 04:52:54 04:52:56 04:52:58

Q. So is it fair to say that one of the reasons why you believe that the term "PCI bus transaction" requires the entirety of the PCI specification is because otherwise execution of the claim doesn't make any sense? 04:53:05 04:53:07 04:53:10 04:53:15 04:53:24

MR. DAVIS: Objection; form. 04:53:26

THE WITNESS: The claim says "PCI bus transaction", PCI is a well-defined standard, so this is basically just already stated right here. That it wouldn't make any sense above and beyond is a different story, but I believe it is sufficient that it says here "PCI bus transaction" and, I mean, we have discussed before that under the broadest reasonable interpretation, this is how it would have to be 04:53:31 04:53:33 04:53:35 04:53:39 04:53:42 04:53:43 04:53:46 04:53:48 04:53:50

interpreted. 04:53:54

BY MR. BUROKER: 04:53:54

Q. In your view for the Horst reference, would any of the address information in that PCI bus transaction that was originated by our PCI device be conveyed to the memory CPU? 04:54:03 04:54:04 04:54:09 04:54:13

A. You mean that some bits of the original PCI transaction ended up being the same at the far end? Is that the message? I'm not sure I understand. 04:54:20 04:54:22 04:54:26 04:54:29

Q. Right, yeah. 04:54:30

A. Well, you have to -- 04:54:31

Q. Not randomly the same. Let me ask it differently. 04:54:33 04:54:36

So the scenario we talked about where you've got a PCI bus transaction that's started by a PCI device and sent up through the pipe towards the CPU and memory, that scenario. 04:54:39 04:54:41 04:54:42 04:54:45

A. Uh-huh. 04:54:48

Q. Would any of the information from the PCI bus transaction that was created, the address information, find its way up through the TNet system to the CPU/memory? 04:54:49 04:54:51 04:54:56 04:55:00

MR. DAVIS: Objection; form. 04:55:04

THE WITNESS: To answer that question 04:55:08

I would have to have a definition of the address 04:55:09
translation in this document -- and I'm pointing 04:55:13
to the Horst reference -- is actually being done, 04:55:15
this is not disclosed at all. There is no 04:55:18
indication, as far as I know, unless you point me 04:55:21
to it and I overlooked it, which says how it 04:55:25
works in particular. It is typically done as 04:55:29
a table lookup, but typically done doesn't mean 04:55:32
it is done like this here or it is obviously to 04:55:35
do it like that. 04:55:37
BY MR. BUROKER: 04:55:41
Q.   And what do you mean by "a table 04:55:41
lookup", what would that mean? Would the address 04:55:43
information in the PCI bus transaction be 04:55:45
included in the TNet -- 04:55:51
A.   No. 04:55:53
Q.   -- packet? 04:55:55
A.   As far as I know, there is no 04:56:01
address translation which is done or even 04:56:06
possible which is functioning through some sort 04:56:09
of an algorithm, right, you calculate the 04:56:12
translated address. There is many reasons for 04:56:18
it. It is always done like that. You have 04:56:21
a particular address which you like to translate 04:56:25
and then there is a bunch of tables which can 04:56:28

have a rather complex form, they can be hierarchical, where the translated address is being searched. Now, what is the granularity of those tables or how the particular searching algorithm works depends on the particular implementation and there is nothing disclosed in Horst, and I therefore don't wish to speculate, but in my declaration I put an example of an address translation which is in the book by Dave Patterson and Hennessy, right? There is a diagram which shows one way it's being done as an example. 04:56:30 04:56:36 04:56:40 04:56:43 04:56:46 04:56:51 04:56:53 04:56:56 04:56:59 04:57:04 04:57:09 04:57:12

Q. Do you know where that is in your declaration? 04:57:13 04:57:15

A. I'm already looking. I got the wrong here, here is '873. Page 20, for example. 04:57:16 04:57:18

Q. Which declaration? 04:57:41

A. '814. 04:57:42

Q. Okay. 04:57:52

A. Before we go into details, one again has to be very clear that an address is only valid if you have all bits. Like a telephone number, if I take off two or three bits of telephone number, the rest of the bits have no meaning, or you need to dial a lot of 04:57:53 04:57:56 04:57:58 04:58:00 04:58:03 04:58:04

numbers before you reach the right number. 04:58:08
The way it is usually being done in 04:58:12
computers, sorry, in processors -- so you are far 04:58:14
outside the TNet context now -- but in case of 04:58:20
a microprocessor there are the address 04:58:23
translation where the main memory is broken up 04:58:29
into so-called pages. The size of a page is 04:58:32
a fixed thing and depends really on the 04:58:35
architecture of the processor, and that has some 04:58:38
reasons which are quite complicated and have to 04:58:41
do with the fact that one tries to make the 04:58:46
address translation as efficient as possible, 04:58:48
allowing it to happen in parallel to the cache 04:58:50
lookup. Typical page sizes are 4 kilobytes. And 04:58:54
that means for every virtual address, the upper 04:58:59
bits beyond the 4 kilobytes are basically that 04:59:02
page number being addressed, right? You could 04:59:08
say page number 0, 1, 2, 3, 4, 5 until you 04:59:12
reached the full space. This is what he calls 04:59:15
the virtual page number. That goes into 04:59:19
a translation scheme. Extremely oversimplifying 04:59:21
you could say this is a table which basically has 04:59:26
as index this virtual page number and as content 04:59:31
the physical page number to which it translates 04:59:35
to. In reality it's not done like that, that 04:59:38

simple, because then these tables would become huge, consuming -- 04:59:42 04:59:45

Q. You're looking at page ... 04:59:50

A. Page 20. 04:59:52

Q. Page 20 of the '814? 04:59:53

A. '814. Ah wait ... yeah '814. There you are but how come it's on the left page in your case? 04:59:55 05:00:14 05:00:15

Q. This is the '873 declaration. 05:00:17

A. Oh, I can also use the '873 declaration, it doesn't matter. Just let me find it here. 05:00:21 05:00:24 05:00:27

Q. Oh, I know why, I'm looking at page 20 of the response, it's my fault. It's been a long day. 05:00:30 05:00:32 05:00:36

Page 20, we're on the same page, 20 of the '814. Okay, I see where you're talking about. 05:00:37 05:00:41 05:00:44

A. So typically this translation scheme are multiple references to main memory of the computer trying to find the right page number, but for the simplicity of the argument you could consider this as a one-step process being a large, large single vector. That means the physical address is assembled by the 05:00:45 05:00:46 05:00:50 05:00:54 05:00:58 05:01:00 05:01:04

translated physical page number and the lower 12 address bits which are the same as the virtual address. This is how a microprocessor does it. This is how basically every processor does it with implementation variance on the translation table itself. And for every process in the system you have an individual private address translation table, meaning for every virtual address scope you have such a table.

Q. Okay, but going back in paragraph 135 of the '814 declaration, you say because:

"... TNet address are virtual addresses ... that TNet address cannot be PCI standard addresses which are physical addresses."

A. Yeah.

Q. But couldn't you just fill in the PCI bus address field into the A field of your TNet packet?

MR. DAVIS: Objection --

BY MR. BUROKER:

Q. 32 bits for 32 bits, you couldn't do that?

MR. DAVIS: Objection; form.

THE WITNESS: What would it help you?

I mean I tried to outline that in a TNet system like that, you have so many different address spaces and every node has its own predefined local physical address space already, right? So, you can't just use any arbitrary PCI address to address something inside this target node because they wouldn't match. That doesn't rule out that under some extreme rare conditions in one particular case there would be a trivial translation, but the general case is certainly not correct. 05:02:31 05:02:38 05:02:41 05:02:45 05:02:51 05:02:57 05:03:02 05:03:06 05:03:10 05:03:13 05:03:15

BY MR. BUROKER: 05:03:16

Q. Well what about in a situation where instead of having multiple CPU memories, like you see in Figure 9, you just had one? So all of the devices on the PCI bus could use an addressing scheme that would map to the memory, the single CPU memory? 05:03:17 05:03:18 05:03:22 05:03:33 05:03:43 05:03:48

MR. DAVIS: Objection; form. 05:03:50

BY MR. BUROKER: 05:03:54

Q. So that you could then use the PCI bus address straight into the TNet address field? 05:03:54 05:03:56

MR. DAVIS: Objection; form. 05:04:03

BY MR. BUROKER: 05:04:05

Q. Is that possible is my question. 05:04:05

MR. DAVIS: Objection; form. 05:04:07

THE WITNESS: I mean you're trying to re-engineer TNet back to a PCI hierarchical single-node system. I would have to consider that. It's not disclosed at all or even suggested in this disclosure here. It wouldn't make much sense to use the system as such. 05:04:11 05:04:14 05:04:19 05:04:24 05:04:27 05:04:31

BY MR. BUROKER: 05:04:39

Q. But your testimony is that what would make sense would be to throw away the address piece of a PCI bus transaction and create a new one. Is that right? 05:04:39 05:04:41 05:04:44 05:04:48

A. To map -- 05:04:50

MR. DAVIS: Objection; form. 05:04:50

THE WITNESS: -- you have to lay out an address scheme for all of the devices involved. In order to implement that you have your address translation. Whether or not in a particular case the translation could be trivial, I don't know it's possible, but it's certainly not the general case and it's certainly not indicated in here, and it would make it unlikely that this system works with a large number of nodes. And still you wouldn't have a PCI transaction in the far end because then 05:04:52 05:04:55 05:04:58 05:05:00 05:05:08 05:05:11 05:05:19 05:05:21 05:05:29 05:05:32 05:05:39

there is just an ordinary CPU. 05:05:41

BY MR. BUROKER: 05:05:51

Q. Right, but in that scenario, if 05:05:52 you took the address information and the data 05:05:53 information out of the PCI bus transaction and 05:05:58 you communicated both of those through TNet 05:06:00 packets up to the CPU/memory, you would have 05:06:03 communicated at least the address and data 05:06:09 information of a PCI bus transaction to 05:06:13 a northbridge, right? 05:06:16

MR. DAVIS: Objection; form. 05:06:17

THE WITNESS: In order to know whether 05:06:28 or not that could possibly work we would have to 05:06:30 really study the details of a particular 05:06:32 processor, the already predefined address maps 05:06:35 inside that system, same for the PCI subsystem. 05:06:39 And if that all would work out and one could 05:06:45 create such an address map, which would be more 05:06:48 like a lucky windfall and only work for a rather 05:06:51 -- like you constructed a single-node system in 05:06:56 my mind -- then you would transmit the 05:06:59 information of the PCI transaction. You would 05:07:05 still not transmit the PCI transaction, the 05:07:08 payload. 05:07:11

BY MR. BUROKER: 05:07:14

Q. Did you know Dr. Horst? 05:07:14
A. No. 05:07:16
Q. Have you ever seen this TNet 05:07:17
article on the IEEE? 05:07:21
A. I did not. 05:07:23
Q. Did you receive IEEE publications? 05:07:25
A. We have them in the library, in 05:07:33
fact I have purchased them, grinding my teeth 05:07:38
because it's really expensive. But there is 05:07:41
a lot of material. I certainly didn't read all 05:07:45
IEEE papers, there's no way I could do that. 05:07:48
Q. Sure. And had you ever heard of 05:07:51
the TNet system? 05:07:52
A. No. 05:07:53
Q. And you knew who Tandy -- Tandy or 05:07:54
Tandem? 05:07:57
A. Tandem. 05:07:57
Q. Tandem Computer Company was, 05:07:59
right? 05:08:01
A. (The witness nodded.) 05:08:01
Q. Had you ever done any work with 05:08:02
Tandem Computer Company before -- well, had you 05:08:04
ever done work with Tandem Computer Labs? 05:08:06
A. Not that I'm aware of. In fact, I 05:08:10
mean for me TNet would have not been something 05:08:15

highly exciting because the reasoning for 05:08:19
developing it is not something I follow to 05:08:26
100 percent because, for example, they argue that 05:08:36
SCI is useless to them because of all the added 05:08:38
complexity of the cache coherency protocols, 05:08:42
neglecting the detail that there is 05:08:45
a non-coherent version of SCI which is exactly 05:08:47
what I have been using, so to me there would have 05:08:51
been no benefit switching technologies. Then 05:08:53
TNet would have been something proprietary by 05:08:55
Tandem. Highly unclear whether or not these 05:08:58
network devices would be sold openly on the 05:09:03
market, which is a strict requirement for us 05:09:06
being able to use this technology. It would be 05:09:10
a sole source. Sole sources are a big problem if 05:09:12
you build these large-scale systems with a plan 05:09:16
15 or 20 years in the future. This is why we 05:09:21
really like standards in this context, therefore, 05:09:24
that was likely for me not to show up on my radar 05:09:28
screen. And if somebody in my contacts would 05:09:31
have seen it, it would most likely not have been 05:09:34
something where somebody would have said, "Hey, 05:09:39
you really have to read this." 05:09:41

MR. BUROKER: I'm about to move to 05:09:49
a different subject, why don't we take a break 05:09:50

and go off the record. 05:09:50

05:09:50

(Volume I of II in the deposition of Volker Lindenstruth concluded at 5:09 p.m.) 05:09:52

- - - - - - -

ACKNOWLEDGEMENT OF DEPONENT

I, VOLKER LINDENSTRUTH, do hereby certify that I have read the foregoing transcript of my testimony taken on 8/27/15, and further certify that it is a true and accurate record of my testimony (with the exception of the correction listed below):

Page Line Correction

____|_______|__________________|_________________

____|_______|__________________|_________________

____|_______|__________________|_________________

____|_______|__________________|_________________

____|_______|__________________|_________________

____|_______|__________________|_________________

____|_______|__________________|_________________

____|_______|__________________|_________________

____|_______|__________________|_________________

____|_______|__________________|_________________

____|_______|__________________|_________________

____|_______|__________________|_________________

____

VOLKER LINDENSTRUTH

SUBSCRIBED AND SWORN TO BEFORE ME

THIS ______ DAY OF ______________, 20___.

____

REPORTER'S CERTIFICATION

UNITED KINGDOM:

I, Audrey Shirley, accredited court reporter, do herby certify that the witness whose deposition is hereinbefore set forth appeared before me in London, United Kingdom on the 27th day of August 2015, at 8:57 a.m.; was duly sworn before the commencement of the deposition; that the testimony was taken down by me using machine shorthand; that all appearances of counsel and participants hereto are noted on the appearance page; and that such deposition is a true, correct, and full record of the proceedings.

I further certify that I am not related to nor employed by any of the parties to this action; that I am not employed by counsel for any of the parties to this action; and that I am in no way interested in the outcome of this matter.

IN WITNESS WHEREOF, I have hereunto set my hand this 27th day of August 2015.

Audrey Shirley

AUDREY SHIRLEY, Court Reporter

'

0

1

2

3

B

C

D

EMC EXHIBIT 1028
EMC v. ACQIS, IPR2014-01462

F

M

Q

S